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SECTION 1 Functional Description

INTRODUCTION

This section is divided into three sub-sections, namely:-

1.2 Rectification techniques

1.3 Technical description

1.4 Circuit diagrams

1.2 RECTIFICATION TECHNIQUES

Introduction

It is assumed that the reader is familiar with the Introduction to Servicing of the 1170 FRA, as explained in section 7 of the 1172 Operating Manual (July 1975 issue). The purpose of this Servicing Manual is to assist the reader in the task of fault rectification, and like any other electronic equipment, fault rectification on the 1170 series is carried out in chronological steps which may be summarised as follows:-

1) Definition:-	The fault is defined in terms of the published specification for the instrument.
2) Diagnosis:-	The faulty or maladjusted components or assemblies are isolated.
3) Replacement:-	Faulty components or assemblies are removed and replaced with serviceable items.
4) Adjustment:-	Any variable components affected by the fault are adjusted to the limits defined in the calibration procedures.
5) Performance check:-	To ensure that the whole instrument is performing within the published specification.

A competent service engineer will find it possible to rectify many faults using standard test equipment and the information contained in this manual. More complex faults, including any which require adjustment after component replacement, will require the use of the special test equipment. A list of this equipment is given in appendix A to this sub-section.

It should be noted that calibration instructions are included as part of the special test equipment and are not given in this manual.

ACCESS

Most parts of the instrument are accessible with ease. Figs. 2.2.1. to 2.2.5. should be consulted to determine the location and method of assembly of the various parts. Extension boards and leads are available (see special test gear list) to enable any board to be worked on in situ.

CAUTION

An extension lead, Type No. TG 1212R, is available allowing operation of the 1172/1177 out of the mainframe. When fitting this lead observe the following procedures:-

1. Switch off power.

2. Fit the cable making sure the plugs and sockets are correctly orientated and secure before switching on the power.

Severe damage may result if the cable is plugged in with power on and incorrect pin mating.

FRONT PANEL TOUCH KEYS

Care must be taken when replacing lamps in these keys. A metal deposition on the glass cover forms the touch plate. This is connected to the circuit by means of the spring clips which also form the cover securing clip. Care must, therefore, be taken that the springs are not distorted and that good contact is made with the plate upon replacement. The contact clip on the touch button cover must be flush with the inner side.

DISPLAY UNIT

If the display unit is to be serviced it is necessary to remove the whole unit and support it clear of the case. Great care must be taken during this operation to ensure that an insulating sheet is placed under the display unit. 200V is generated within the display unit. **This voltage can destroy parts of the instrument or cause injury to the user, if great care is not taken.**

FAULT DIAGNOSIS

For the purposes of fault diagnosis and rectification the instrument may be regarded as consisting of several major functional areas.

The following block diagram defines these major areas.

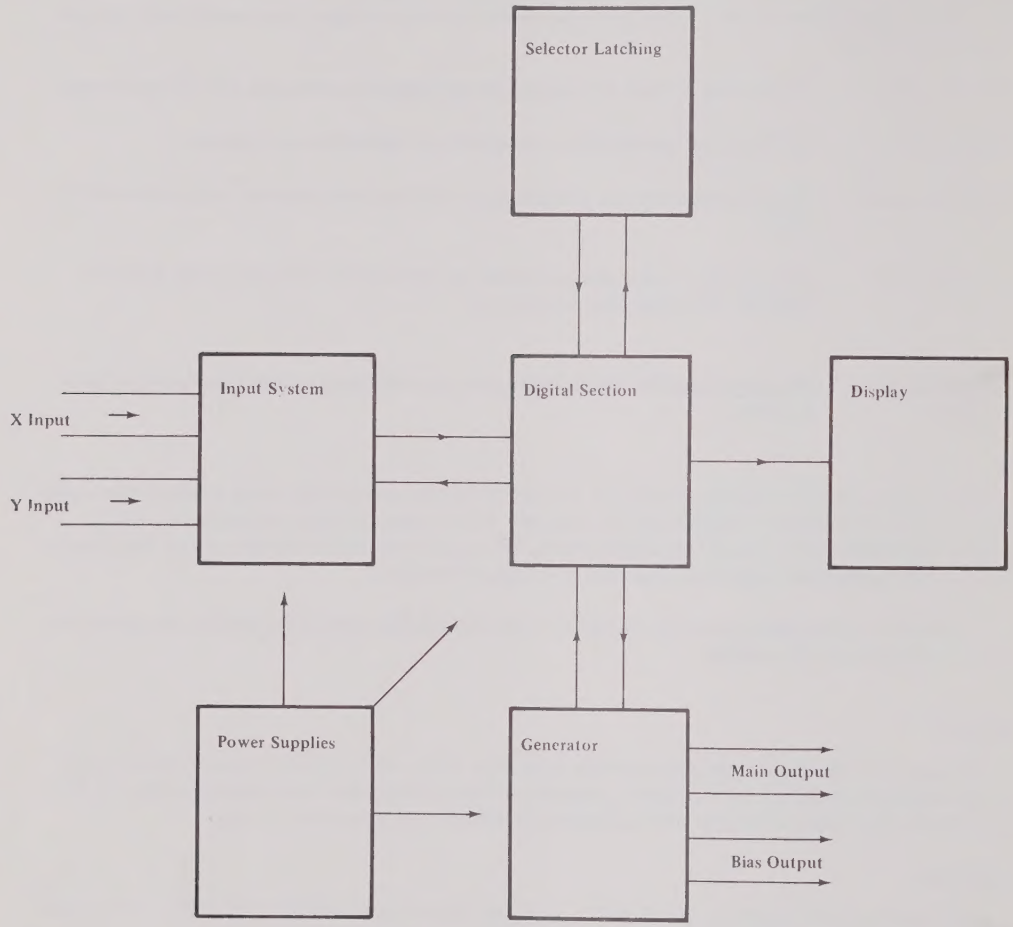


Fig. 1.2.1

Reference should be made to the 1170 Circuit Diagram Allocation Chart, which appears in both Sections 1 and 2, where all circuit diagrams and printed circuit boards for each of the areas are listed.

The type of fault diagnosis that may be attempted depends, to a large extent, upon in which of the areas the fault falls.

An item of special test equipment is available which assists in fault location; namely the Store State Indicator Type TG1212A.2, available from your Schlumberger agent. See Appendix B.

When the faulty area has been located, rectification action will vary between the areas. A description of the recommended treatment for each area is given in the following paragraphs.

POWER SUPPLIES

Fault finding may be carried out using traditional methods in this area. After rectification a certain amount of re-calibration may be required. Care must be taken when working on these circuits to preserve the isolation of the floating supplies. In particular, the 0V rails must not be interconnected between the earthy and floating sections.

INPUT SYSTEM

Servicing in this area requires use of the techniques used on most high accuracy measuring instruments. Signals may be followed using standard test equipment. It must be remembered that this is a floating section and that the precautions normally taken in these circumstances must be observed.

The control of the circuits in this area originate in the digital section, coupling between the earthy and floating section being made by optical couplers.

This area contains many variable components. Therefore in many cases re-calibration will be required after fault rectification.

DISPLAY

This area consists of a 200V generator, together with several neon indicating devices and associated decoding circuits. Servicing of this area is straight-forward but the decoding circuit will require careful study when diagnosing the more obscure faults.

No calibration of this area is necessary.

SELECTOR LATCHING

This area consists of an unconventional loop circuit best explained by the following diagram.

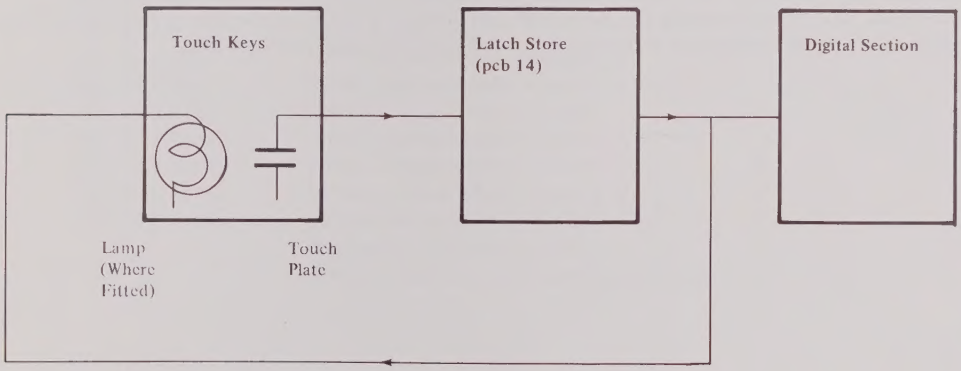


Fig. 1.2.2

When a touch button is touched, the appropriate latch store location is activated. The digital section uses this latch store information to perform the necessary actions; it is also passed back to the touch button, causing the lamp to light.

The data from the front panel are serialised before being passed to the latch store for decoding. The feed-back data is also in serial/parallel form.

Although fault-finding is possible, using standard test equipment, familiarity must be gained with the timing sequences used, before the data can be interpreted intelligently.

The most useful item of test equipment for use in fault finding is the Store State Indicator, and its use is strongly recommended. With this instrument one can examine the contents of any latch store location, or write-in a new selection without using the front panel. Intelligent use of the SSI will usually quickly establish the cause of a fault.

DIGITAL SECTION

This area is an arithmetic processor, digital store and digital control circuit. It uses techniques similar to those used in digital computers and the service technician should therefore be familiar with these techniques.

Attempting to follow signals through the circuits of this area will often prove abortive, and although simple faults may be diagnosed using standard test equipment, it is recommended that Complete pcb replacement is used to rectify the more complex faults.

To carry out an efficient repair service on this area it is therefore desirable to carry a spare set of serviceable pcb's No. 2, 3, 4, 5, 7, 8, 10, 11, 12, 13, 15, 16 and 17. A Store State Indicator TG1212A.2 as used in the Selector Latching area is also recommended.

Determination of the faulty board or component within this area will often require a combination of:-

1) An exammination of the contents of the appropriate MOS store locations by means of the SSI.

2) A knowledge of the operation of each of the pcb's.

3) An intelligent interpretation of the indications of unserviceability, as shown by the effects on other areas of the instrument.

4) In certain cases, a degree of trial-and-error by substituting pcb's and observing the effect. This must, of course, be used with discretion to avoid causing further faults.

5) If a second 1170 FRA of known serviceability is available, a rapid method of fault location by means of pcb exchange between the two instruments may be used. Care must of course be exercised to prevent damaging the serviceable instrument. For this reason this method should not be used if a fault is suspected to be in the power supplies or associated circuitry.

APPENDIX A Special Test Equipment

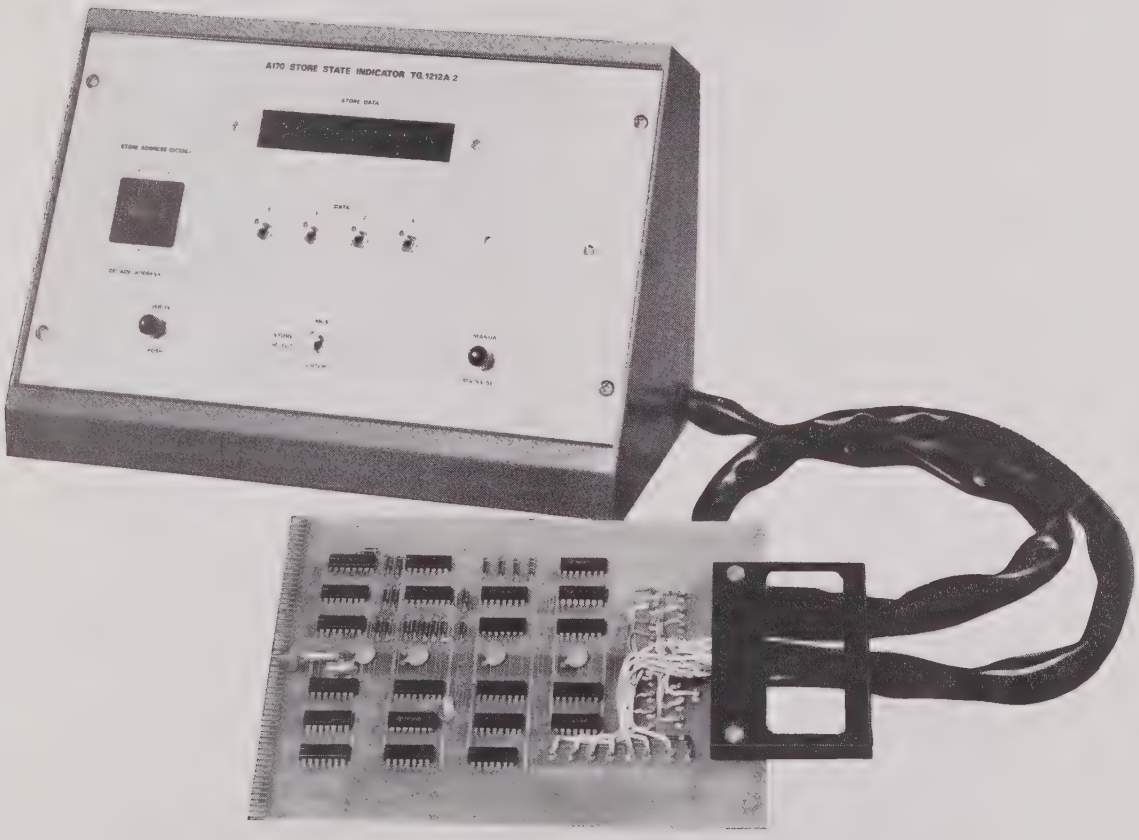
TYPE No.	NOMENCLATURE
TG 1212A.2	Store State Indicator
TG 1212 BB	Square Wave Calibrator Unit
TG 1212 CC/1	Straight through
TG 1212 CC/2	20 db Attenuator
TG 1212 CC/3	40 db Attenuator
TG 1212 CC/4	60 db Attenuator
TG 1212 CC/5	1184 90° Phase Unit
TG 1212 CC/6	Fundamental Rejection Filter
TG 1212 CC/7	Harmonic Rejection Filter
TG 1212 D/18	P. Supply Lamp Monitor Board
TG 1212 D/22	Carries P.S. Lamp Monitor and Leading board
TG 1212 D/23	Input system Lamp Monitor and Leading board
TG 1212 IA	A170 Extension board
TG 1212 IB/1	A172 Extension board (24 way)
TG 1212 IB/2	A172 Extension board for Bd 11 (with additional inverter protection Resistors - for fault finding).
TG 1212 IB/3	D-A Programme board - simplified
TG 1212 C	A172 Extension board - 16 way
TG 1212 L	Display Test Set
TG 1212 P	P. Supply Pulse Driver (position PCB 26)
TG 1212 R	A170 - A172 Extension Lead
TG 1212 T	Relay timing unit
TG 1212 X/3	5 volt loading board - 4 amps
TG 1212 X/9	5 volt loading board - 4 amps
TG 1212 X/13	5 volt loading board - 4 amps
TG 1212 X/16	5 volt loading board - 4 amps
TG 1212 X/14	5 volt loading board - 8 amps
TG 1212 X/19	18 volt leading board - 3 amps
TG 1212 X/20	18 volt leading board - 8 amps
	Production Test Specification (Full calibration instructions and testing)

APPENDIX B1 Store State Indicator

Introduction

This instrument is an item of test equipment used for fault diagnosis and calibration of the 1170 series of Frequency Response Analyser.

The 1170 contains two major storage systems, called respectively the MOS store and the Latch store. The Store State Indicator (SSI) enables the contents of these stores to be examined and data to be written directly into them.



A170 Store State Indicator

SSI OPERATING INSTRUCTIONS

Principle

The eight LED numerical indicators continuously read the data held in selected locations of the MOS or Latch stores. If "MOS" is selected the display will show the contents of the eight locations of the group selected by the first and third thumbwheel selector switches. If "Latch" is selected the data held in two locations will be displayed. In this case the data will be displayed four times in alternate windows. A complete list of selections is given later, in tabular form.

The second thumbwheel switch and the four data switches are used to write-in new data as an alternative to the use of the FRA front panel.

Applications

The SSI has two main applications; fault location and calibration.

For fault location the SSI is used to read the contents of the stores directly so by-passing the FRA display or touch-key indicators. Data may also be directly inserted into the stores from the SSI, so by-passing the touch-keys and, in certain cases, parts of the arithmetic and measuring systems.

It is impossible to list all the instances in which these facilities may be used but after some practice the operator will soon realise its full usefulness.

For calibration purposes the SSI has two facilities which make it almost indispensible. Firstly it may be positioned so that the duplicated display may be viewed from the rear of the FRA, where the adjustments are made. Secondly, the SSI displays two more significant digits than the FRA display. The FRA in its arithmetic processor computes to two decades more than are displayed or specified. The viewing of these two digits by the SSI enables the operator to make setting-up adjustments to a higher degree of accuracy than by the use of the FRA display alone.

Before using the SSI it is necessary to acquire a working knowledge of the stores.

The MOS Store

The store is IC5 on pcb No. 12 of the 1170. The circuit is found on Diagram No. 66. It contains a maximum of 256 four bit words.

In this store are contained all the results of the various computations made during the correlating process, together with the parameters of voltage and frequency commanded from the front panel.

The SSI allows the contents of eight of the locations to be read at one time or data to be written into one of them. The location to be written into or the group to be read is selected by the Selector switches which form an assembly of three octal coded thumbwheel switches, allowing selection of 0 to 377_8. (0 to 255 in decimal notation). Conversion from octal to decimal radices is explained later.

A table showing the contents of the various locations is given later, together with the SSI operating procedures.

The Latch Store

This store occupies most of pcb No. 14 and part of pcb No. 16 of the 1170. The storage elements are D type flip-flops and are found on Diagrams 32 to 36.

The store contains data which defines all the selections made on the front panel touch buttons. (The required measurement parameters are held in the MOS store).

The SSI allows the examination of any of these locations and the direct writing-in of data.

A table of the switch selections necessary, and the contents of the store is given later, together with the operating procedures for the SSI.

Timing

Access is made to the various locations of both stores by means of strobe pulses originating in the SSI.

Each of the 256 locations of the MOS store is connected to the 4 input and 4 output busses, in turn, by a 500kHz clock. A synchronising pulse is used to begin each 256 pulse sequence. The timing of the strobe pulse is decided by the settings of the selector switches. Thus the selection indicates the time slot allocated to each of the locations. This information is of use if it is desired to view the bus data by means of an oscilloscope.

The selection is in octal code. It is therefore necessary to convert to decimal and count from the synchronising pulse to identify a location. For instance, Table 1, shows that the 3rd digit of θ (Y) in radians is found on selection 264 (= 180 dec). This location will therefore be connected to the busses 180 pulses at 500kHz after the synchronising pulse.

The same sequence of 256 pulses that are used to clock the MOS store are used for the Latch store. But in this case only the first 16 pulses are required.

The timing sequence, which, it will be noted, is the reverse of the address switch selection is as follows:-

1st pulse. **No. 7 of second column (Harmonic selector) of Table 2.**

↓

8th pulse. **No. 0 of second column (Sweep mode)**

↓

9th pulse. **No. 7 of first column (Sweep command)**

↓

16th pulse. **No. 0 of first column (Integration time)**

Operating Instructions

Installation

It is recommended that the SSI interface board is plugged into position 18 of the 1170 although position 20 may be used if 18 is occupied. No other connections to the SSI are required. The 1170 power switch should be off when the SSI is inserted.

Operating Procedures

MAINS SET - Operation of this switch sets all stores to the state at power switch-on. It must not therefore be operated unless this state is intended.

MOS/LATCH selector - Operating procedures after this selection is made differ slightly. They are therefore treated under separate headings.

MOS

Refer to Table 1. To read the data in a group of store locations select on the first and third bank of the selector switch the required numbers. The data contained in the location for each of the eight digits will be shown in the appropriate window.

5th and 6th Significant Digits

The display of each measurement by the 1170 is to four significant digits, but it will be noted that the SSI displays the same data to six significant digits, the last two being used for correlation proceses but not displayed.

Write-in

To write-in data the first and third selector switches must be set to the appropriate group, and the centre switch set to the digit into which new data is to be written.

The data is then set on the four data switches.

Switch Up = 1
Switch DOWN = 0

e.g. To write-in value 6:- SW8 ↓, SW4 ↑, SW2 ↑ and SW1 ↓.

Next press and release the *write* button and observe that the data shown in the selected digit window has changed to the new value.

Unused Addresses

The addresses marked N.U. may contain data, but interpretation is impractical. Address 0n0 may contain data if an 1185 Synchroniser is fitted. The other addresses contain temporary data used in the computation processes.

Latch

As the latch store occupies only 16 locations,the first of the Store Address selector switches is not used and can remain on any selection.

To read the contents of a location, only the third selector switch need be set, when the contents of two locations will be observed simultaneously. Care must be taken when reading, as each item of data is repeated four times in alternate windows. *Table 2* lists the locations and an interpretation of the data they may contain.

Write-in

As well as the third Selector switch, to write-in, the second (Decade Address) must also be set to either 1 or 0, depending on in which column the required location appears in table 2. Also "Remote" must be selected on the FRA front panel.

The data to be written in is then set in BCD on the four data switches,

Switch UP = 1
Switch DOWN = 0

e.g. To write-in the selection —ve BIAS, the data value 6 must be inserted into the Keyboard group location, which (from Table 2) requires the selection of X11 on the thumbwheel switches. The data (6) is then selected:- SW8 ↓, SW4 ↑, SW2 ↑, SW1 ↓.

The "write" button is then pressed and the display observed to check that the data has changed in the four appropriate windows. i.e. windows 0, 2, 4 and 6 will show 6 in the case used as the example.

Input Range

Selections 5 and 6 require some care when reading or writing. Location 5,0 contains data on the input range in use by the 1170. The data can only be input to this location via selection 6,0. Location 6,0 contains data showing whether a fixed range or auto is selected. Therefore if any fixed range is selected,this store (6,0) will only show data 0 but location 5,0 will show the actual range. If auto is commanded location 5,0 will show the range in use.

Octal to Decimal Conversion

Take octal number 5 2 3 4

$= 4 \times 8^0 = 4 \times 1 =$ 4
$= 3 \times 8^1 = 3 \times 8 =$ 24
$= 2 \times 8^2 = 2 \times 64 =$ 128
$= 5 \times 8^3 = 5 \times 512 =$ 2560

2716

$\therefore 5234_8 = 2716_{10}$

Octal weightings

$8^0 =$ 1
$8^1 =$ 8
$8^2 =$ 64
$8^3 =$ 512
$8^4 =$ 4096
$8^5 =$ 32768
etc.

Octal to Binary

$1_8 =$ 001
$2_8 =$ 010
↓
$7_8 =$ 111
$10_8 =$ 001 000
↓
$77_8 =$ 111 111
etc.

MOS STORE

Notes to Address Chart

1. To read. Select 1st and 3rd Switch selection [Store Address (Octal)]. The eight windows show the data held in the selected location.

2. To write. Select 1st and 3rd Switch selection. Select digit to be written into on 2nd switch (Decade address). Select data value (up = 1 down = 0). Press "write" switch.

3. On table 1:-

   1 = Most significant digit

   2 = 2nd

   3 = 3rd

   4 = 4th (Least significant digit of display)

   5 = 5th

   6 = Least significant digit in store

   Ex = Exponent. The value is given in "notes"

   O/L = Overload

4. Shaded digits. Any data shown in these spaces should be ignored.

5. Notes on individual addresses.

   1n0 to 3n2 — These are measured values held in the stores (except those not used, n.u.)

   0n3 — Add Bias. As commanded from front panel.

   1n3 — Log f. The logarithm of the data held in location 2n7.

   2n3 — V_{OUT} (DISP) The value (numbers only) commanded from front panel (See 0n7).

   3n3 — Bias (Rej) As measured when "input reject" is commanded. This value is not displayed on 1170.

   1n4 to 3n5 — Measured values.

   0n6 to 3n6 — Frequencies as commanded from front panel.

   0n7 — V_{OUT}(OP) The generator output voltage.

   2n7 — f_{OUT}(OP) The generator output frequency.

   3n7 — Δf_{LOG}. Number of measurements per decade as commanded from front panel.
   377 is Mains set command when written-in.

CONTENTS	SWITCH SELECTION	n		NOTES
N.U.	0	0		1185 Period Data
R (X)	1	0	1 2 3 4 5 6 Ex	Ex 2 = xx.xxxx O/L 4 = x.xxxxx V 6 = xxx.xxx V etc
R (Y)	2	0		
R (Y/X)	3	0		
N.U.	0	1		
a (X)	1	1	1 2 3 4 5 6 Ex	Ex as R
a (Y)	2	1		
a (Y/X)	3	1		
N.U.	0	2		
Log R (X)	1	2	1 2 3 4 5 6	
Log R (Y)	2	2		
Log R (Y/X)	3	2		
ADD BIAS	0	3	1 2 3 4 5 6	
Log f	1	3	Ex Ex 1 2 3 4	Ex. 04 = 1Hz to 10Hz 07 = 1kHz to 10kHz etc.
VOUT (DISP)	2	3	1 2 3 4	
BIAS (REJ)	3	3	1 2 3 4 5 6	Ex. as R POL. 1 = Rej. + ve 0 = Rej. -ve.
N.U.	0	4		
θ (X)	1	4	1 2 3 4 5 6 Ex	
θ (Y)	2	4	Degrees Minutes	
θ (Y/X)	3	4		
N.U.	0	5		
jb (X)	1	5	1 2 3 4 5 6 Ex	Ex as P
jb (Y)	2	5		
jb (Y/X)	3	5		
fMAX	0	6	1 2 3 4 Ex	Ex. 1 = x.xxx mHz 4 = x.xxx Hz 7 = x.xxx kHz etc
fMIN	1	6	1 2 3 4 Ex	
f (DISP)	2	6	1 2 3 4 Ex	
Δ fLIN	3	6	1 2 3 4 Ex	
VOUT (OP)	0	7	1 2 3 4 Ex	Ex. 1 = .01V Range 2 = 0.1V 3 = 1V
N.U.	1	7		
f (OP)	2	7	1 2 3 4 Ex	Ex as fMAX
Δ fLOG	3	7	1 2 3 4 M.SET.	Write M.SET to clear all stores.

TABLE 1. MOS STORE ADDRESS CHART (Before use see notes)

3rd switch selection	COLUMN 1 **To write**, select 0 on Decade Address, with third Store Address switch as shown on left. **To read**, select third Store Address as shown and read windows:- 		COLUMN 2 **To write**, select 1 on Decade Address, with third Store Address switch as shown on left. **To read**, select third Store Address as shown and read windows:- 	
0		**Integration Time** 0 MIN 1 x 10 2 x 100 3 x 1000		**Sweep Mode** 0 LIN 4 LOG
1		**Measurement Delay** 0 MIN 1 1 2 10 3 100		**Keyboard** 0 f_{MIN} 1 f_{MAX} 2 f_{REQ} 3 f_{INCR} 4 O/P V 5 + ve BIAS 6 – ve BIAS
2		**Display Co-ordinates** 0 Polar (R*0*) 1 Cartes (A + jB) 2 LOG R*0*		**Frequency Range** 0 mHz 1 Hz 2 kHz
3		**Measure** 0 X - Y (not used) 1 X 2 Y 3 Y/X		**Generator Mode** 0 Ramp 1 Sine 2 Square
4		**Measure Sequence** 0 Stop 1 Re-cycle 2 Single 3 Stop (end of cycle)		**Carrier Modes** 0 Normal 1 Mod O/P 2 Demod I/P 3 Mod O/P Demod I/P
5		**Input Range** 2 10mV 3 100mV 4 1V 5 10V 6 100V Read Only		**Bias Mode** 0 Normal 1 Add bias 2 Reject bias 3 Add & Reject bias
6		**Input Range** 0 Fixed 2 10mV 3 100mV 4 1V 5 10V 6 100V 8 AUTO Write Only		**Local/Remote** 0 Local 8 Remote (If Local is written-in, no further data can be written until Remote is commanded on front panel).
7		**Sweep Command** 0 OFF 1 HOLD 2 UP 3 DOWN		**Harmonic Selector** (Used with extension units)

TABLE 2. LATCH STORE ADDRESS CHART

1.3 TECHNICAL DESCRIPTION

This section, when read in conjunction with section 1.4, provides a description of the instrument in both a theorectical and functional form.

An introductory section describing the various processes used in the 1170 system is followed by a functional description of the instrument, using block diagrams with direct reference to the circuit diagrams. This serves to describe the analogue parts of the instrument, the digital sections being described in a mainly theoretical fashion at the end of this sub-section.

INTRODUCTION TO MACHINE ORGANISATION

Note: 1177 readers should ignore any references to SWEEP or BIAS.

The 1170 is divided into two parts - the "Generator" section and the "Analyser" (correlator) section.

The Generator section produces an electrical sine wave output signal. The amplitude and frequency of this signal are controlled from the keyboard.

The Analyser accepts an electrical input signal, and, when commanded from the keyboard, makes a measurement on this signal and displays the results.

Measurements may be made on either of two input channels (channel X or Y), and the most recently measured results on either channel (X or Y), or the ratio between them (i.e. "point to point" result, Y/X) may be displayed. The results may be displayed in any of three co-ordinate systems (A and jB, R and θ, or log R and θ).

The instrument contains a data store (MOS STORE), in which are stored all the results, as well as the generator operating parameters, the frequency sweep parameters and the bias generator output voltage. It also contains an "arithmetic unit", which is used to calculate the results, and a "control logic" section, which controls the overall sequence of operations performed by the machine.

The generator parameters, frequency sweep parameters and bias voltage may be altered from the keyboard when the instrument is not measuring. Some action by the control logic and arithmetic unit is necessary when changing the generator parameters - the frequency sweep parameters and bias voltage may be changed directly via the keyboard. Any one of these parameters may be displayed in the "Keyboard Display", by touching the appropriate key.

The "Results Display" can display any one set of results from the store in accordance with the setting of the A, B; R, θ; log R, θ and X; Y; Y/X keys.

MEASUREMENT SEQUENCES

The simplest measurement which the machine can make is made with the following front panel touch key settings:

Sweep OFF

SINGLE Measurement

Channel X

Reject Bias OFF

Fixed input voltage range

To make a measurement under these conditions, the input is first analysed by the "*correlation*" process (see CORRELATION IN THE 1170). This gives an intermediate result, which, after division by "integration time", T (by the arithmetic unit), provides results in A, jB form which are placed in the MOS store. Further calculation by the arithmetic unit gives the single channel results in the other co-ordinate systems, which are also stored. The "point to point" results are then calculated and stored, using the previously measured results for channel Y from the store.

The other functions which can be provided by the instrument, when requested from the touch keys, are accomplished as follows:

1. Autorange	Measurement starts on the 10mV range. If the instrument overloads, the measurement is terminated immediately, the input range is increased by a factor of 10, and a new measurement commenced. This is repeated, if necessary, until the 100V range is reached.
2. Reject Bias.	A measurement is made in the "Measure bias" mode. The single channel calculation proceeds to the point where the in-phase component (real part) is known. A voltage of this magnitude is then generated internally and applied as a "backing-off" voltage to oppose the bias, and a new measurement taken.
3. Point to point.	A set of relays ("input relays") is provided so that the input of the analyser can be connected either to the channel "X" terminals or to the channel "Y" terminals. A channel "X" measurement is taken and the single channel results calculated and stored. The input relays are then changed to channel "Y", and another measurement taken, and single channel and point to point results calculated and stored.
4. Frequency sweep.	Before the measurement, a new frequency is calculated by the arithmetic unit, using the parameters which have been entered into the store from the keyboard (f MIN, f MAX, Δ f LOG, Δ f LIN). The generator frequency is changed to this new frequency. A delay depending on the setting on the "measure delay" touch keys is then allowed to elapse before commencing the measurement. This allows any transient in the "system on test", due to the change in frequency, to die away.
5. Recycle	A continuous series of measurements is initiated. Between each measurement, a delay is allowed to elapse depending on the setting of the "measure delay" touch keys.

INTRODUCTION TO THE GENERATOR

The Generator section of the instrument generates a sine, square or triangular waveform stimulating signal which is used to excite the system under test.

Clock Generator

This section of circuitry consists essentially of a synthesizer employing an R.F. varactor - tuned oscillator and a first order programmable phase-locked loop. The output is a clock frequency of 2000f (200f on the 10kHz range) where f is the required output frequency.

The clock is utilised by the generator to produce the sine wave output, and also by the arithmetic system to produce the sine and cosine signals required for correlation. A number of crystal controlled fixed frequencies are also produced for use throughout the system, e.g., 10MHz, 1MHz, 500kHz, 200kHz and 100kHz.

Waveform Generator

An up/down counter and D.A.C. produce an analogue ramp which is converted by means of a seven section shaping network into a low-distortion sine wave of fixed amplitude. Provision is made to produce ramps or square waves by changes of operation. Only one output waveform shape can be produced at any one time.

Bias and Output Volts Control

This converts two pulse sequences, derived from the store data for output volts and bias, into two dc levels, using a precision integrator and two sample/hold circuits.

Programmable Attenuator

This is effectively a multiplier, one input being the fixed amplitude signal from the waveform generator, the other being the dc level proportional to the required output voltage from the bias and output volts control.

Output Amplifiers

These produce the necessary voltage and power to drive the system under test (up to 40V p.p in ac carrier mode, and up to 100mA load current).

Modulators

When systems employing ac carrier modulated signals are measured, the output signals have to be multiplied by a sine wave (carrier reference). The 1184 Mod/Demod Unit converts this reference sine wave into a binary signal with mark/space modulation, and two mark/space multipliers are used in the generator to produce modulated outputs.

Power Supplies

The 100kHz clock output from the clock generator drives an inverter which, via a transformer and bridge rectifiers, produces all the voltage levels to operate the generator.

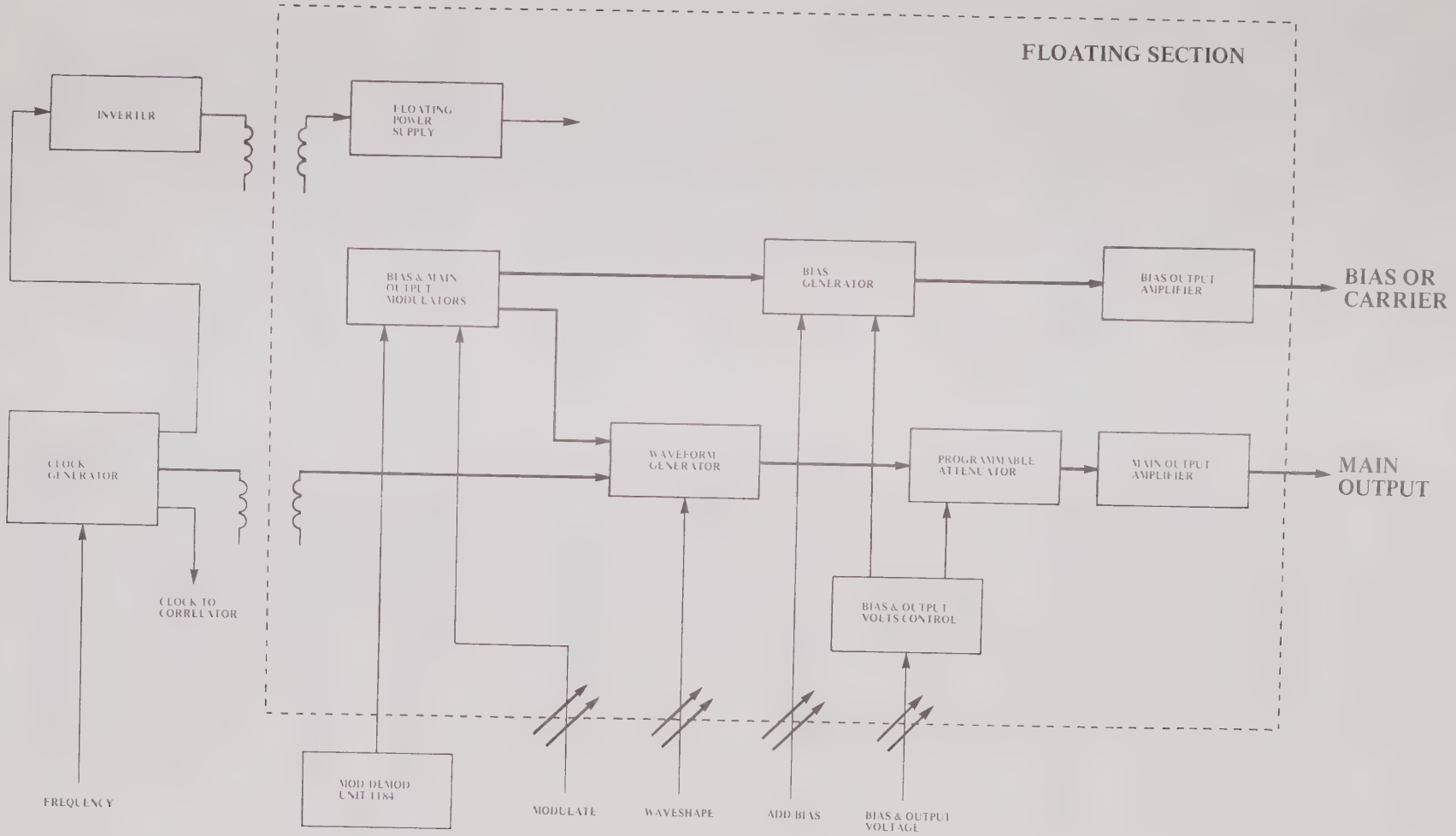


Fig. 1.3.1 BLOCK DIAGRAM - 1172 GENERATOR

FUNCTIONAL DESCRIPTION

The functional description is based upon the following block diagram, which forms the highest level of description.

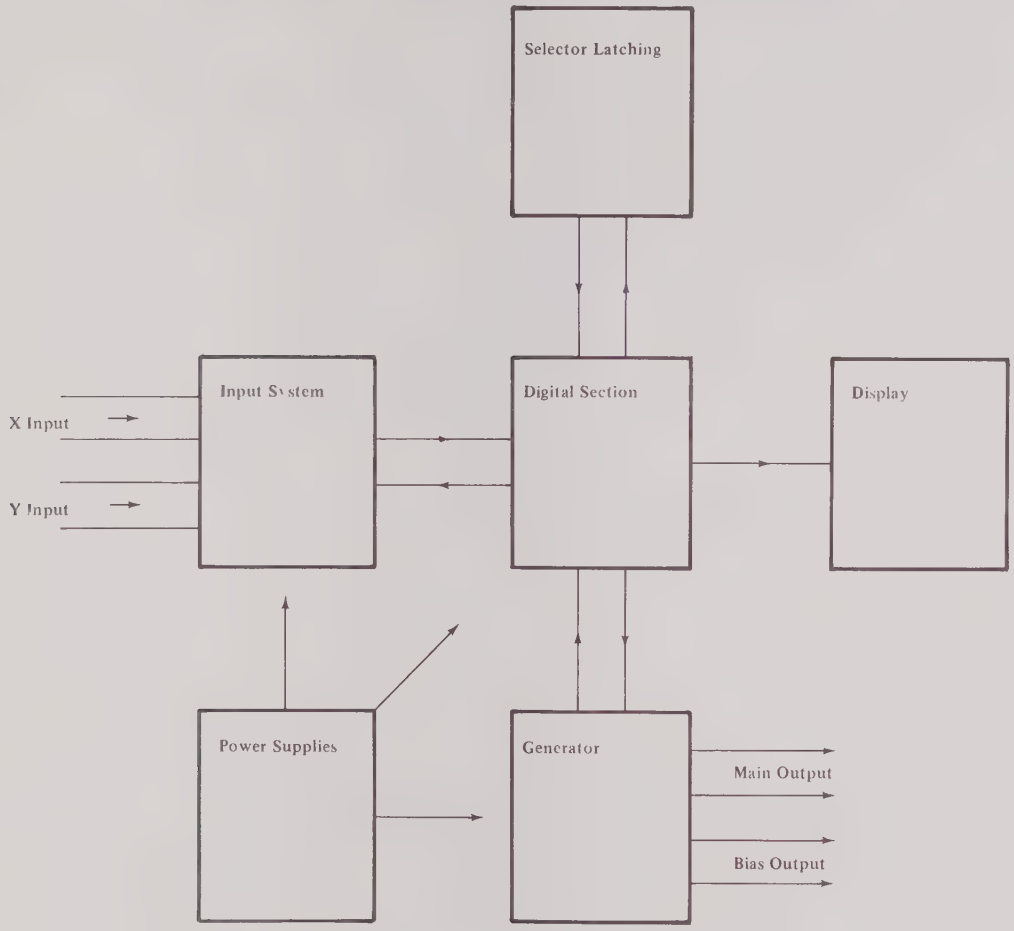


Fig. 1.3.2

The second level takes each of the areas shown in the first level diagram and breaks it down into a series of block diagrams, which make direct reference to the circuits and physical interconnections.

The third level of description is the circuit diagrams proper found in section 1.4. Where necessary a description of the circuit diagram, and a list of its connections with others, is given on each opposite page to the circuit diagram.

Due to its complexity and the nature of its signals it is not possible to cover the digital section in the same way as the others. For this reason a theoretical description of the digital section is given after the functional description. The description is mathematically orientated and uses terms and descriptions used in the design of digital computers. This description is of limited use in a servicing environment but should be studied if a full understanding of the working of the 1170 is required.

The display system is shown as an adjunct to one of the digital section block diagrams.

BLOCK DIAGRAMS

Except for the two diagrams showing the digital section, the block diagrams are arranged in a common format. Each block represents a circuit diagram, the number of which heads the text within the block, the name of the diagram and the numbers of pcbs illustrated in the diagram then follows. Except where indicated by arrows, the main functional paths flow left to right across the diagram. Annotated numbers on the connections indicate the signal in the main interconnection list (Section 2.4.).

Control functions enter the blocks from top, bottom, left or right. The boxed annotations indicate:-

1. The circuit number to which they are connected.

2. The pcb number to which they are connected.

3. The signal name.

4. The interconnection number (in brackets) relating to the list in section 2.4.

Instead of circuit numbers some connections show the following:-

1. DIST. Indicates that it is connected to several circuits.

2. PERIPH. It is connected to one of the peripheral units in positions 18 to 22.

3. DISPLAY. Connected to the display.

POWER SUPPLIES ⟶

All supplies are derived from a +30V unregulated rail in Circuit No. 42. Voltage regulators in Circuit No. 43 are controlled by the sensing amplifiers in circuit No. 45.

The sensing amplifiers in circuit No. 45 are switched at 25kHz, by a clock which is derived from the floating supplies, circuit No. 44, which is in turn driven by a 100kHz clock from circuit No. 2 (in the 1172).

Protection circuits are shown in circuit No. 43.

The mains set signal although not part of the power supply circuit is included as it is distributed via pcb No. 26, the power supply regulator board.

MAINS POWER SUPPLY

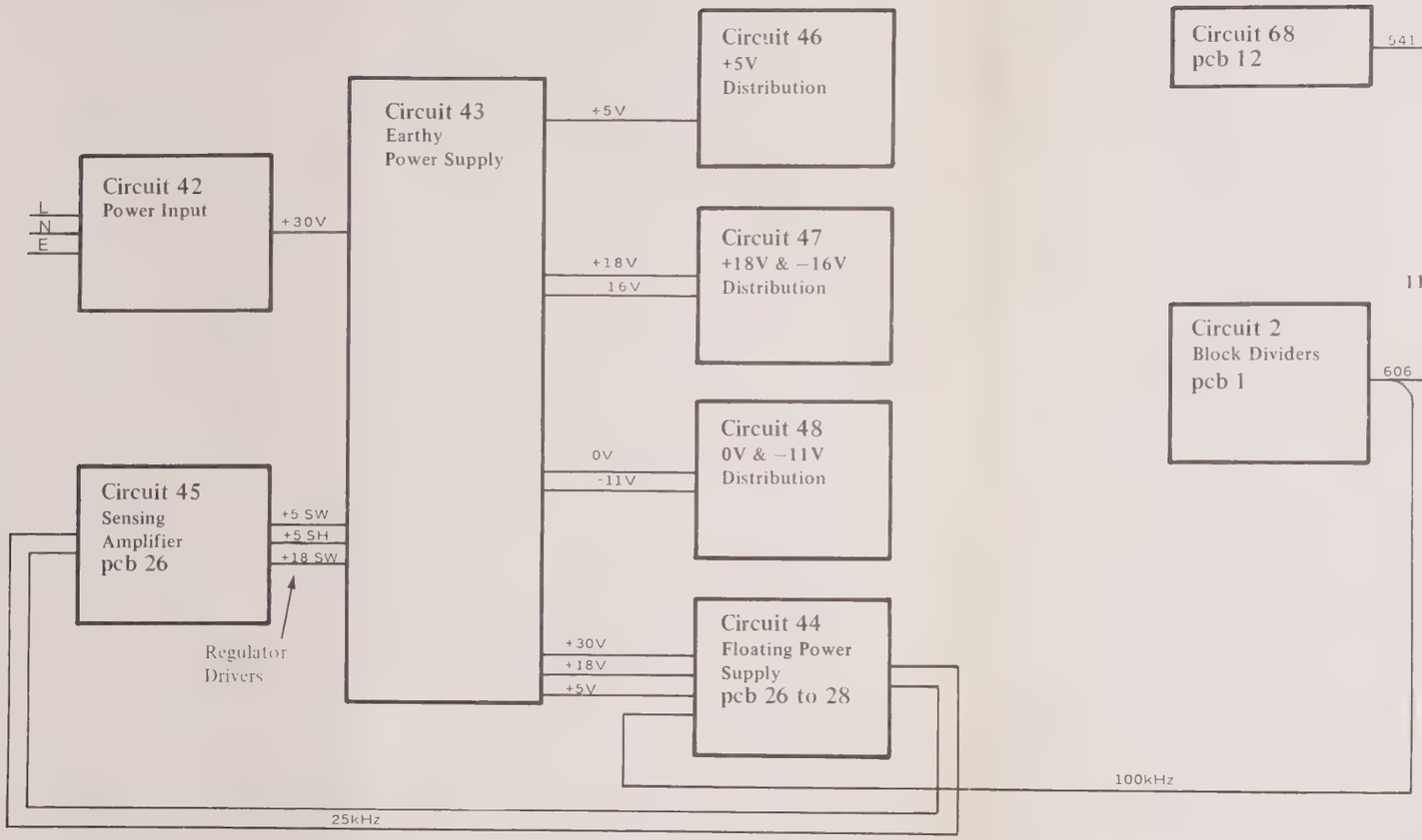
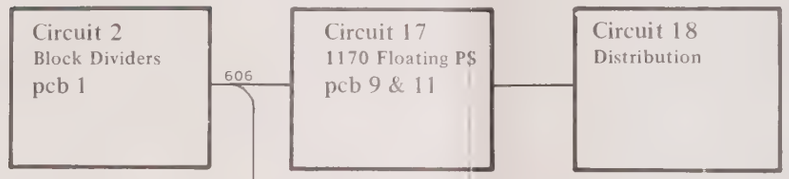


Fig. 1.3.3

MAINS SET SIGNAL

1172 FLOATING POWER SUPPLY



POWER SUPPLIES

GENERATOR, SYNTHESISER

This area has two main functions. Firstly it is used to provide the fixed frequency clocks used throughout the system and secondly to provide the working frequency related to that at which the measurement is to be made, (the synthesiser output frequency).

Fixed clock frequencies are generated by division of a 10MHz crystal oscillator in Circuit No. 1.

The synthesiser output frequency is generated by mixing the output of the fixed 10MHz oscillator with that of a voltage controlled oscillator (VCO) also in Circuit No. 1. The VCO is controlled by a phase locked loop consisting of Circuits No. 3, 4, 5, and 1.

The required synthesiser output frequency is called from the digital section into Circuit No. 3 by the T10 and T9 control lines (543 and 542). When the required synthesiser output frequency is correct the loop is phase-locked and the output of Circuit No. 3 is at 100Hz.

If the synthesiser output frequency is not correct the comparison made between T9, T10 control lines and the VCO output (6.19, 620 into circuit No. 3) will not produce 100Hz. The effect is to produce an increasing or decreasing ramp voltage at the output of circuit No. 5 which is used in circuit No. 1 to adjust the VCO and so bring the loop into phase-lock.

An example of the waveforms which produce the frequency adjustment is shown in Fig. 1.3.4.

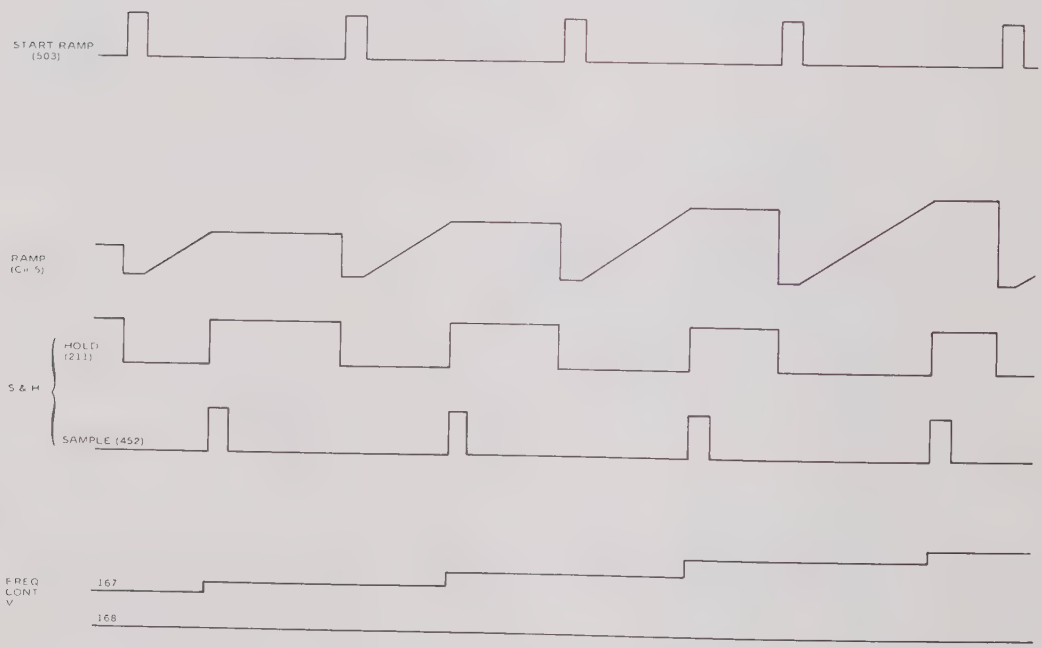


Fig. 1.3.4

In this example the frequency is low, causing the output prf of circuit 3, the samle and hold, to be below 100Hz. The start ramp signal from circuit No. 2, is fixed at 100Hz. The effect is, as shown, a low voltage to the VCO causing its output frequency to increase.

The increasing control voltage causes the synthesiser output frequency to increase until the output of Circuit No. 3. the sample and hold signals. is at 100Hz and the loop is phase-locked.

When the loop is phase-locked the synthesiser output frequency is 2000f (where f is the frequency at which measurement is being made).

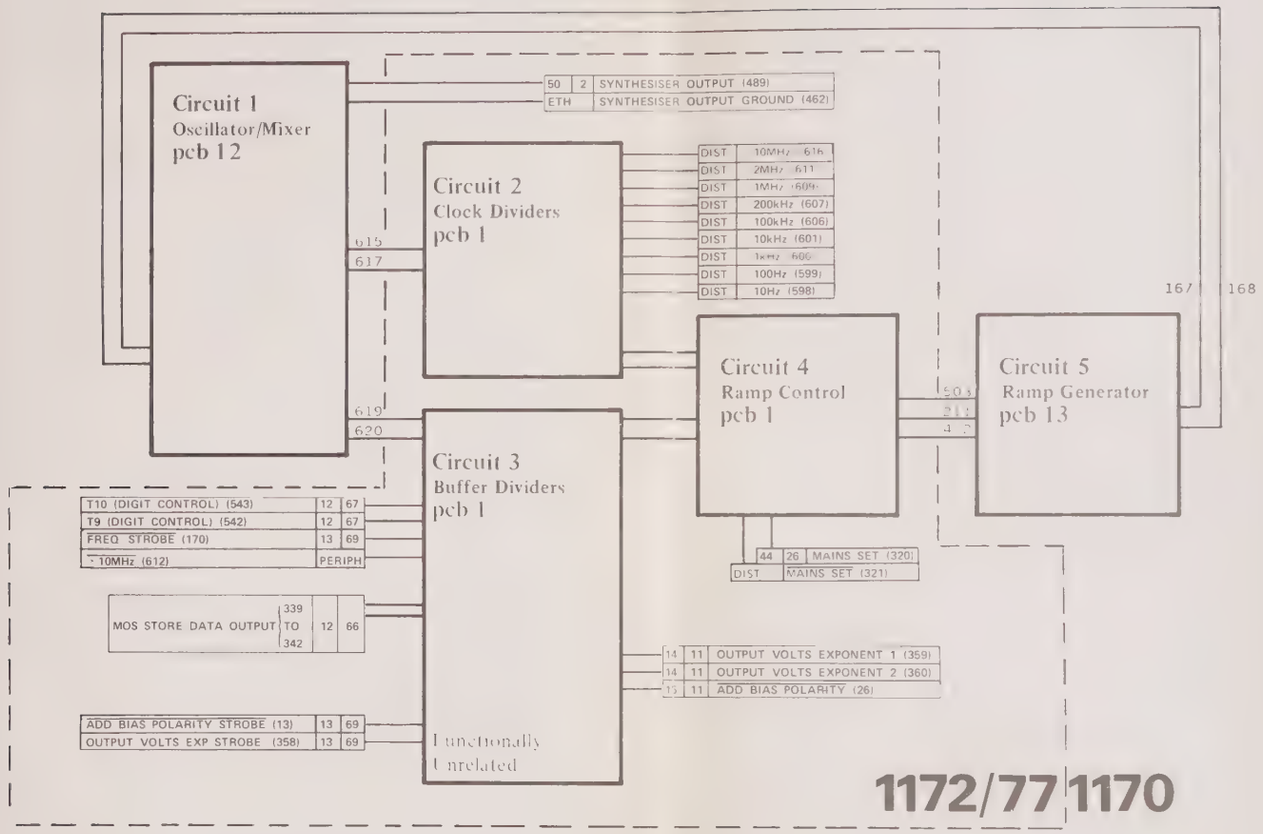

Circuit 1
Oscillator/Mixer
pcb 12
Circuit 2
Clock Dividers
pcb 1
Circuit 3
Buffer Dividers
pcb 1
Circuit 4
Ramp Control
pcb 1
Circuit 5
Ramp Generator
pcb 13
50 2 SYNTHESISER OUTPUT (489)
ETH SYNTHESISER OUTPUT GROUND (462)
615
617
619
620
DIST 10MHz (616)
DIST 2MHz (611)
DIST 1MHz (609)
DIST 200kHz (607)
DIST 100kHz (606)
DIST 10kHz (601)
DIST 1kHz (600)
DIST 100Hz (599)
DIST 10Hz (598)
167
168
503
T10 (DIGIT CONTROL) (543) 12 67
T9 (DIGIT CONTROL) (542) 12 67
FREQ STROBE (170) 13 69
10MHz (612) PERIPH
MOS STORE DATA OUTPUT 339 TO 342 12 66
ADD BIAS POLARITY STROBE (13) 13 69
OUTPUT VOLTS EXP STROBE (358) 13 69
44 26 MAINS SET (320)
DIST MAINS SET (321)
14 11 OUTPUT VOLTS EXPONENT 1 (359)
14 11 OUTPUT VOLTS EXPONENT 2 (360)
15 11 ADD BIAS POLARITY (26)
Functionally
Unrelated
1172/77 1170

Fig. 1.3.5

GENERATOR - OUTPUT SYSTEM

The generator system of the 1172 or 1177 is fully floating, all control from the 1170 Mainframe being by transformer or optical coupling.

Two separate generators, Main and Bias, are provided. During carrier modes of operation, with an 1184 unit fitted, both outputs can be modulated at the carrier frequency.

Some of the control function lines are carried to several of the circuit diagrams. The distribution of three of these is shown in the inset diagram. The change of interconnection number as the function passes through a circuit is shown; and it must be remembered that the signal may be inverted by a circuit.

OPERATION

Voltage Control (Circuit 12)

This circuit, by time sharing Mark/space operation, provides voltage control of both Main and Bias outputs. Output 363 is an analogue voltage used to control the main attenuator. Outputs 24 and 25 are also analogue voltage (+ and — respectively) are used to provide the bias output. (See "Digital to Analogue Conversion").

MAIN GENERATOR

The Generator clock (185) to circuit No. 8 at a frequency of 2000f (or 200f) is fed to circuit No. 9 which provides a parallel digital number proportional to the instantaneous value of the waveform. A D to A converter and shaper in circuit No. 10 uses this number to produce an output of the required shape (sine square or triangular) at frequency f. at a fixed amplitude. (See "Waveform Generation").

The carrier, if required, is added to circuit No. 11 and the signal is passed for attenuation in circuit No. 13. Final attenuation, or amplification to determine the voltage range of the output, is made in circuit No. 14.

BIAS GENERATOR

The polarity of the analogue output of circuit No. 12 is selected in circuit No. 15 and then, if selected, chopped at the carrier frequency.

The output of circuit No. 15, which is either a dc (+ or —) or an ac voltage at carrier frequency, is amplified in circuit No. 16 to provide the bias output.

Digital to Analogue Conversion

The voltage control circuit (12) generates analogue voltages from a digital source in circuit 72 (signal Nos. 186, 187). The system is time-shared with other parts of the instrument and comprises a signal consisting of a series of six MARK - SPACE sequences each proportional to a required analogue voltage, a RESET signal and SAMPLE signals.

Fig. 1.3.6 illustrates two facilities, O/PV control and ADD BIAS.

Operation

Each receiver (in this case circuit 12) shares the D/A RESET and D/A MS signals, which are used to reset an integrator and to control the time during which it ramps respectively. At a fixed time each receiver gets a unique SAMPLE signal. Each SAMPLE signal occurs at the completion of its corresponding MS signal (there are eight sequential MS signals). At this time the voltage reached by the integrator will be proportional to the sum of the mark periods. This voltage is sampled and held. It is continuously updated at each received SAMPLE signal for that particular facility.

The circuit implementation used results in the integrator ramping in a negative direction, thus the voltages which are sampled and held are negative.

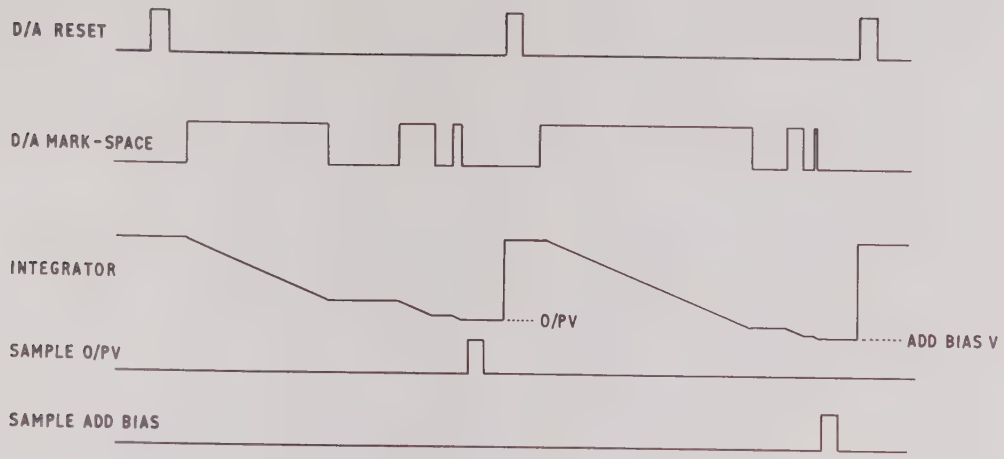


FIG. 1.3.6

Waveform Generation

The output waveform is generated from a digital signal originating in circuit No. 50 in the form of a variable clock. This is used to generate a counter output to circuit No. 10. The counter varies continuously from zero to 500 and back to zero to provide a triangular staircase waveform which defines two quadrants of the output waveform. This waveform is then filtered and shaped to provide the final required waveform.

The waveform is illustrated in Fig. 1.3.7. In practice there are 10 lines which provide 500 steps before reversing the count.

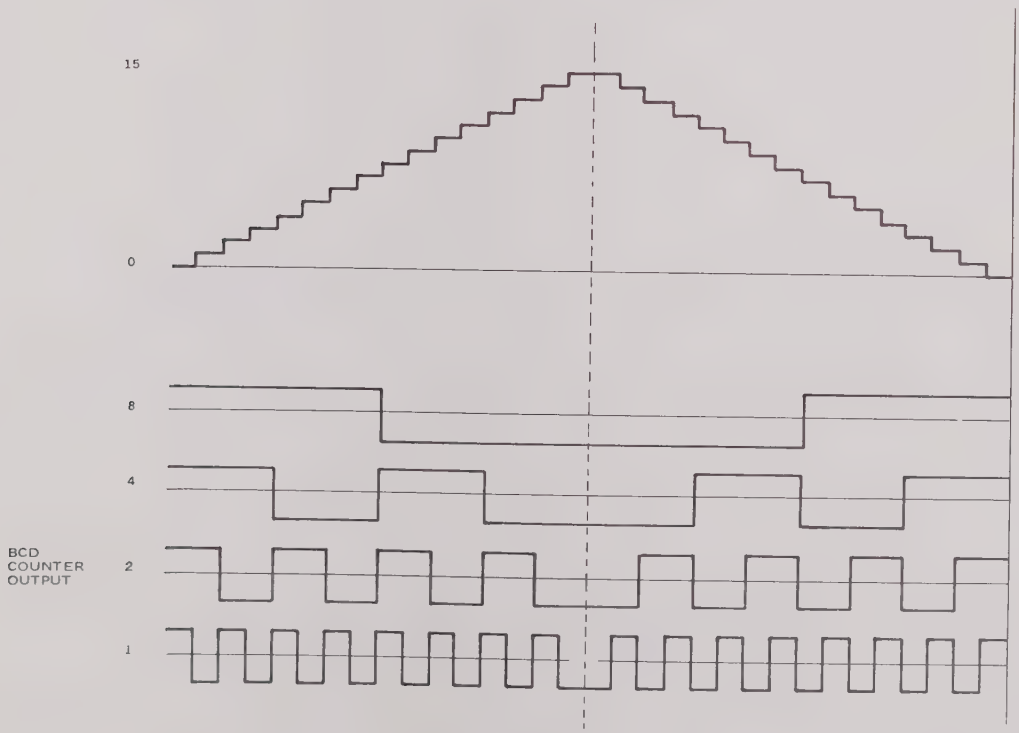


Fig. 1.3.7

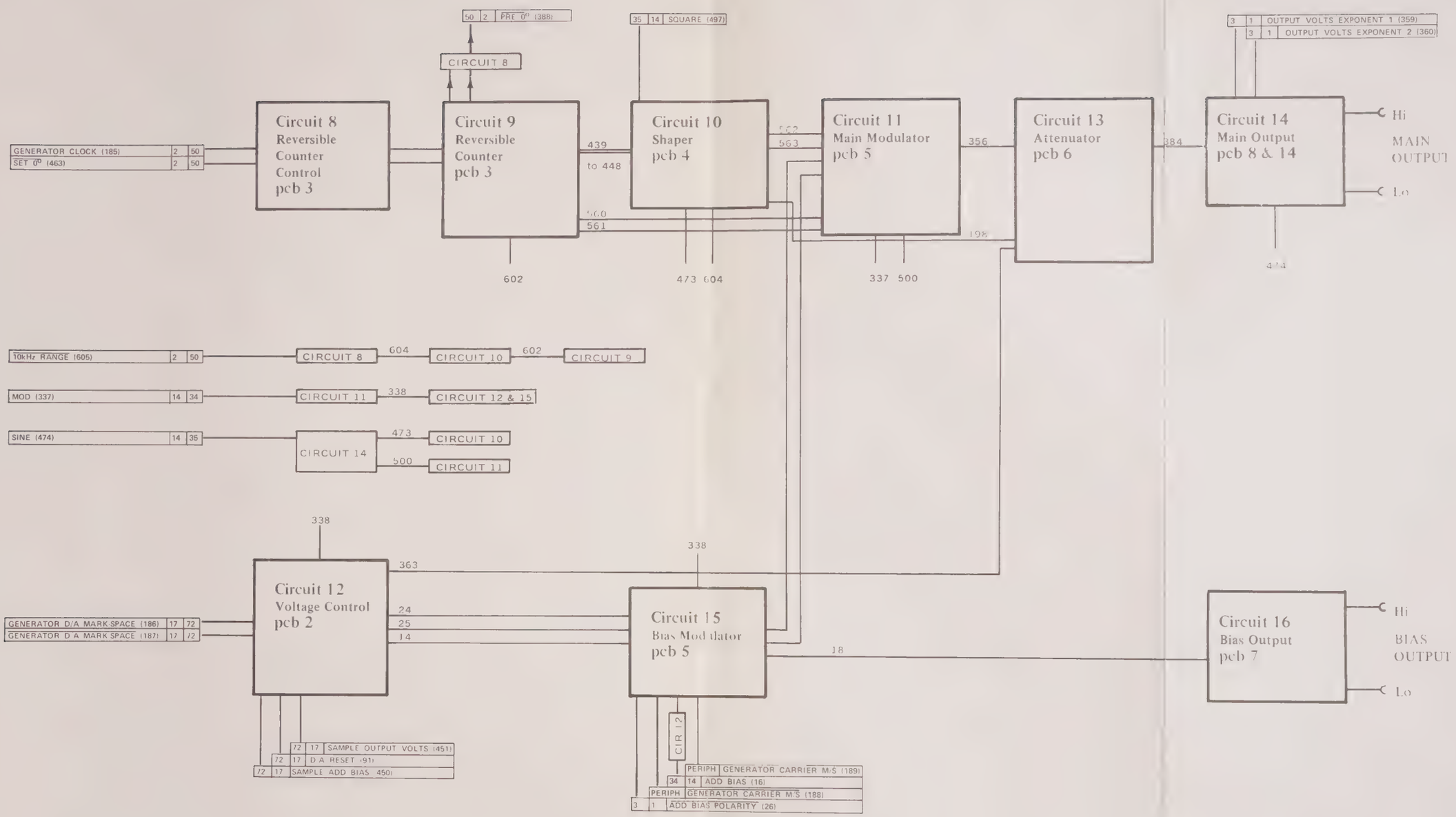


Fig. 1.3.8

GENERATOR, OUTPUT SYSTEM – 1172/1177

INPUT SYSTEM

The input system comprises six circuit diagrams which may be divided into two groups. Circuits 19. 20 and 21 form the measurement circuit and circuits 22, 23 and 24 the bias reject generator.

Before attempting to understand the input system certain facts regarding the operation of the 1170 must be recapitulated. They are:-

1. A measurement is made on only one input (X or Y) at a time.

2. A voltage will be measured, and the result stored, at only a single frequency at a time. Components of the input at any other frequency will be rejected.

3. A measurement cycle consists of one or more complete periods at the measurement frequency.

MEASUREMENT SYSTEM

Measurements are made using an analogue to digital converter using voltage to frequency conversion Fig. 1.3.9 illustrates the principle.

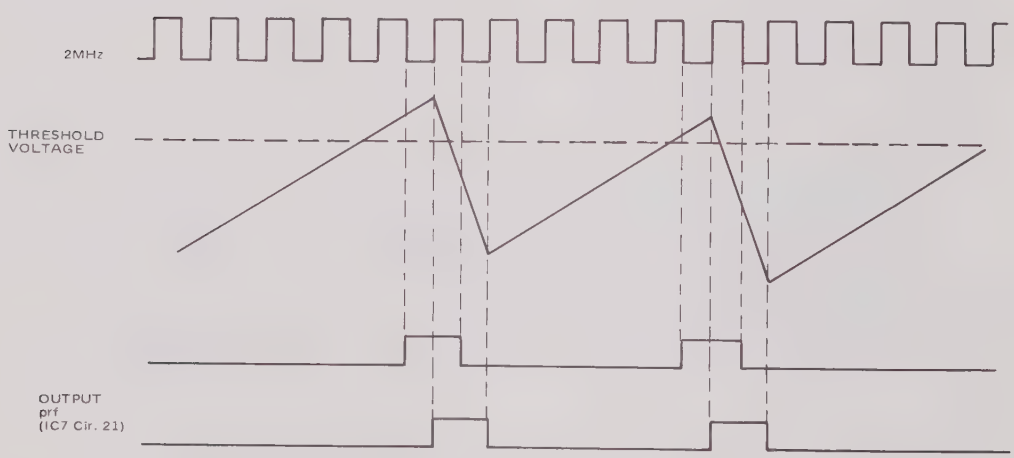


Fig. 1.3.9

The input voltage is, after suitable scaling for range, applied to an integrator, the output of which is a ramp with a slope proportional to the input voltage. When the ramp reaches a certain fixed threshold level a clock causes a pulse to be generated and the ramp to rapidly ramp down and restart. The pulse repetition frequency is therefore proportional to the instantaneous input voltage and will vary with the instantaneous input voltage over the mesurement period.

A theoretical description of the use to which this pulse train is put will be found under the heading "Correlation in the 1170".

The input system, however, does far more than carry out this simple V to F operation. It also:-

1. Rejects any bias contained in the input voltage, whether dc or, in the case of a modulated signal, ac.

2. Demodulates a modulated ac system.

3. Reduces the frequency of signals above 1kHz by heterodyning.

Any combination of the above modes of operation may be used simultaneously.

All three input modes are achieved by means of the CHOP (66) signal to circuit 21. The principle used in all modes is to change the frequency so that its fundamental component is proportional to the value to be measured.

If "bias reject" is selected a two-stage measurement operation is used. Firstly the bias is measured and secondly the signal is measured whilst a backing-off voltage, equal to the previously measured bias, is added.

As an example of the method refer to Fig. 1.3.10.

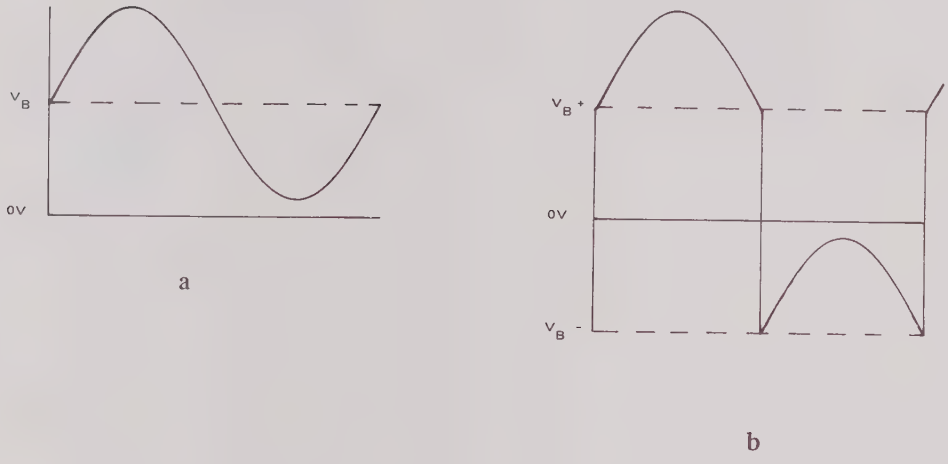


Fig. 1.3.10

Fig. a illustrates a typical input signal with bias (V_B). The FRA measures this bias by chopping the whole signal at the measurement frequency, *f*. The result is as shown in Fig. b. If this waveform (b) were analysed it should be found that the component at the fundamental frequency, *f* is proportional to the original bias voltage, V_B. The original signal voltage has, however, changed in frequency (to mainly 2*f*). The 1170 will only measure the component at *f*, which is scaled to equal V_B.

When the FRA has finished measuring this bias voltage the measurement cycle is started. In this cycle circuits 22 to 24 are used to generate a dc voltage equal and of oposite polarity to the previously measured bias. At the same time the measurement of the signal is made with, of course, the CHOP signal removed.

(Note:- The chopping is done by switching current signals into the V to F converter, thus signals such as that illustrated above cannot actually be observed as voltage waveforms).

DEMOD

During ac carrier operation, when use is made of an 1184 Mod/Demod unit the CHOP signal is used to demodulate the input signal. This is a single-stage operation with the CHOP signal at the carrier frequency. The result is illustrated by the oscillograms of Fig. 1.3.11, which shows an input before and after chopping. (This action takes place as the switching of currents into the V to F converter, and cannot be easily observed with an oscilloscope as voltage waveforms).

a b

Fig. 1.3.11

HETERODYNE

The FRA measures signals below 1kHz. Inputs between 1kHz and 9.999kHz are reduced before measurement by heterodyning, using the CHOP signal. The chopping frequency is, in this case, $\frac{50f}{51}$. The resulting measurement is made at $f - \frac{50f}{51} = \frac{f}{51}$

CHOP FREQUENCY

Any combination of modes is permissible. A list of all possibilities follows, showing the composition of the chopping frequency in each case. The chopping waveform is a digital and the frequencies shown are fundamental frequencies.

CHOP (66) signal frequency

Mode	Measure Bias (1)	Measure Input
Basic	NU	Nil
Basic + DC Bias Reject	f	Nil
Basic (> 1kHz)	NU	$\frac{50f}{51}$
Basic (> 1kHz) + DC Bias Reject	$\frac{f}{51}$	$\frac{50f}{51}$
Modulated Carrier	NU	f_c
Mod. Carrier + Carrier Bias Reject	$f_c + f ; f_c \quad f$ (2)	f_c
Mod. (> 1kHz) Carrier (3)	NU	$f_c + \frac{50f}{51} ; f_c - \frac{50f}{51}$ (2)
Mod. (> 1kHz) Carrier + Carrier Bias Reject (3)	$f_c + \frac{f}{51} ; f_c - \frac{f}{51}$ (2)	$f_c + \frac{50f}{51} ; f_c - \frac{50f}{51}$ (2)

NU Measurement not made

f = Measurement frequency

f_c = Carrier frequency

(1) This signal only exists whilst the bias is being measured, which is only for a period equivalent to the minimum integration time, at the start of each measurement.

(2) These are double sideband signals, they cannot be checked with a counter.

(3) This mode is not normally used as the input system is not correctly scaled for amplitude.

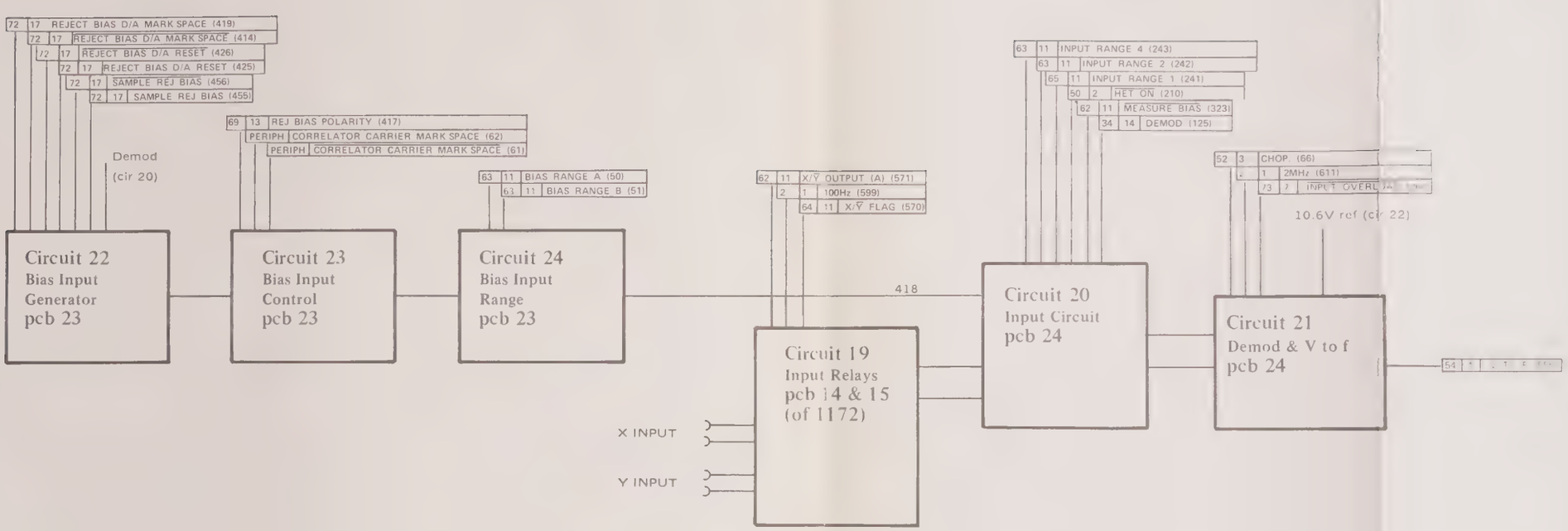


Fig. 1.3.12

INPUT SYSTEM

SELECTOR LATCHING

This section describes the action which takes place when a front panel touch key is touched.

Due to the complexity of the circuit not all the interconnections are shown on Fig. 1.3.13. The connections between pcb's 14 and 16 and the rest of the 1170 are shown in figure 1.3.14 which is an appendix to this diagram. Circuits 25 to 30 and 38 to 41 must be studied to find all the interconnections between them.

OPERATION

There is no direct connection between the touch key itself and the illuminating lamp. In operation, touching a key inserts data into the Latch Store in the 1170. The lamp behind the key indicates that that item of data is held in the Latch Store. When servicing this circuitry it is, of course, important to remember that these keys do not operate in the same way as a conventional illuminated push switch.

The touch keys in circuits No. 26 to 28 are scanned sequentially, in groups, by strobe pulses generated in circuit No. 25. When a touched key is detected a signal is passed to circuit 29. This bit of data will pass out of circuit No. 29 in the form of a pulse in a particular time slot of a 256 bit sequence.

The serial data are decoded in circuit 31, where instructions will be passed to insert the data into either a particular location of the Latch Store, (circuits 32 to 36) or, in the case of numerical data, to the keyboard store, (pcb 15). The keyboard store is not shown on this diagram but is included as an output of circuit No. 36. Block diagram, figure 1.3.15 shows the relationship of pcb 14 to the keyboard display system.

The output of the Latch Store is in a 4 line parallel/serial form. The first 16 time slots of the 256, used for serial data, are used to define the group of latch store data, and the 4 line parallel data the actual latch. The location of each bit of data will be found in the instructions for the use of the Store State Indicator.

The latch store output data are decoded, by use of the strobes from circuit No. 25, to illuminate the appropriate lamp, in circuits No. 38 to 41. For instance, reference to the SSI instructions reveal that the 9th time slot (address X07) contains "Sweep command" information. If at this time the value 2 (0010) is held on the 4 lines the sweep up (↑) light will illuminate.

Some of the latch store data are not carried on the 4 line bus as shown, but on separate single lines. These are shown on the individual circuits.

CIRCUITS 32 to 36

The storage devices used to hold the front panel selections are "D" type flip flops.

Data are written - in by a clock pulse which is formed by a combination of a write strobe and a data pulse. The data that is written is generated in block FLA of circuit No. 31 (D inputs to the flip-flops).

The store locations are best understood if the instructions for the use of the Store State Indicator are referred to. Table 2 of the SSI lists the Latch Store locations. The following table relates this information to the hardware.

Contents of the stores are read in sequence by the read strobes generated in block FRA of circuit 31.

Store Location	Function	Circuit No	Block	PCB	IC
0 - 0	Integration time	32	FLB	14	34
0 - 1	Measure delay	32	FLC	14	34
0 - 2	Display	32	FLD	14	29
0 - 3	Measurement	32	FLE	14	29
0 - 4	Measure Sequence	33	FLF	14	36
0 - 5	Input Range	73	–	17	30
0 - 6	Input Range	73	–	17	30
0 - 7	Sweep Command	33	FLG	14	32
1 - 0	Sweep Mode	33	FLH	14	39
1 - 1	Keyboard	36	FLO	16	36
1 - 2	Frequency Range	35	FLM	14	42
1 - 3	Generator Mode	35	FLL	14	42
1 - 4	Carrier Mode	34	FLJ	14	11
1 - 5	Bias Mode	34	FLK	14	22
1 - 6	Control	35	FLN	14	24

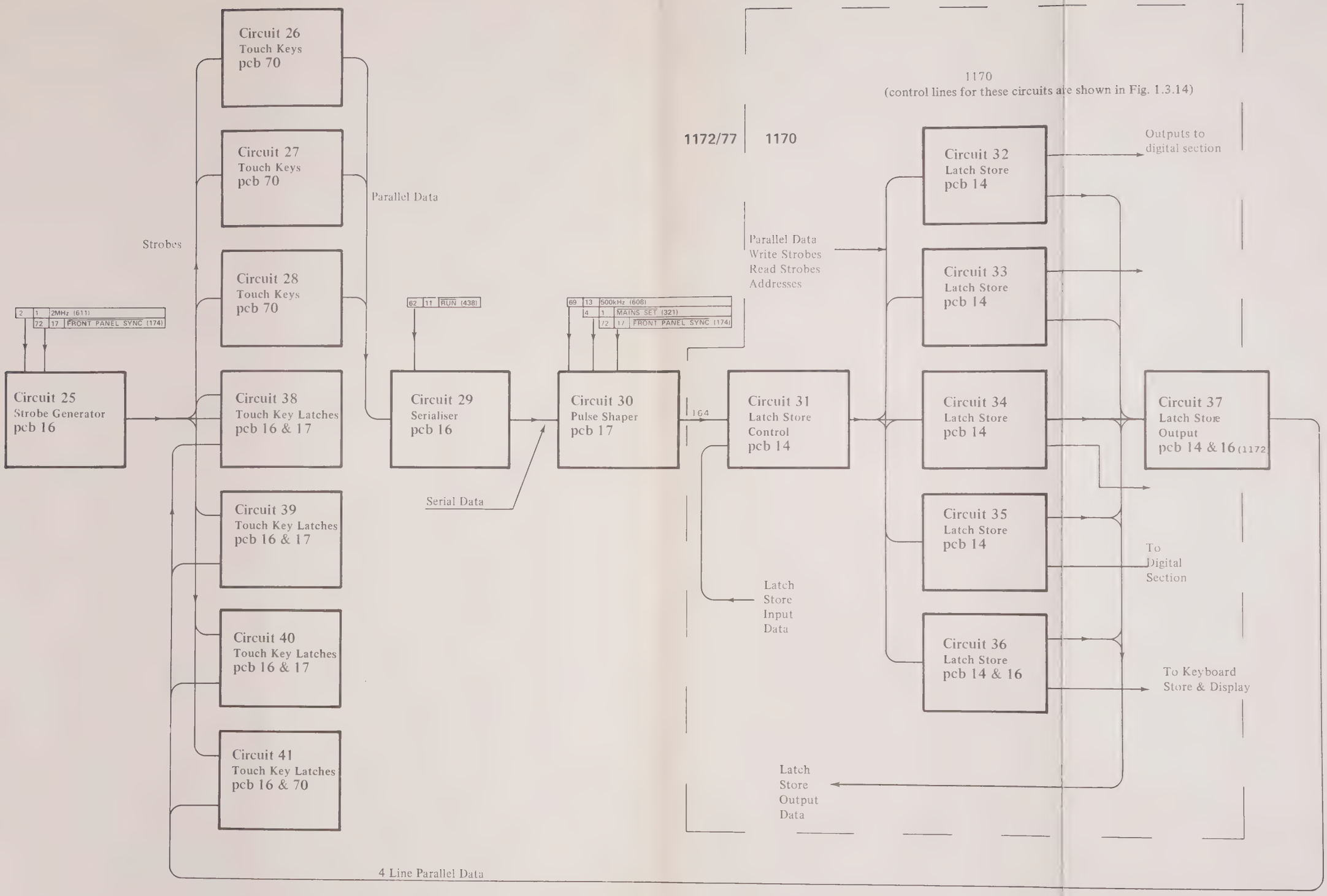


Fig. 1.3.13

SELECTOR LATCHING

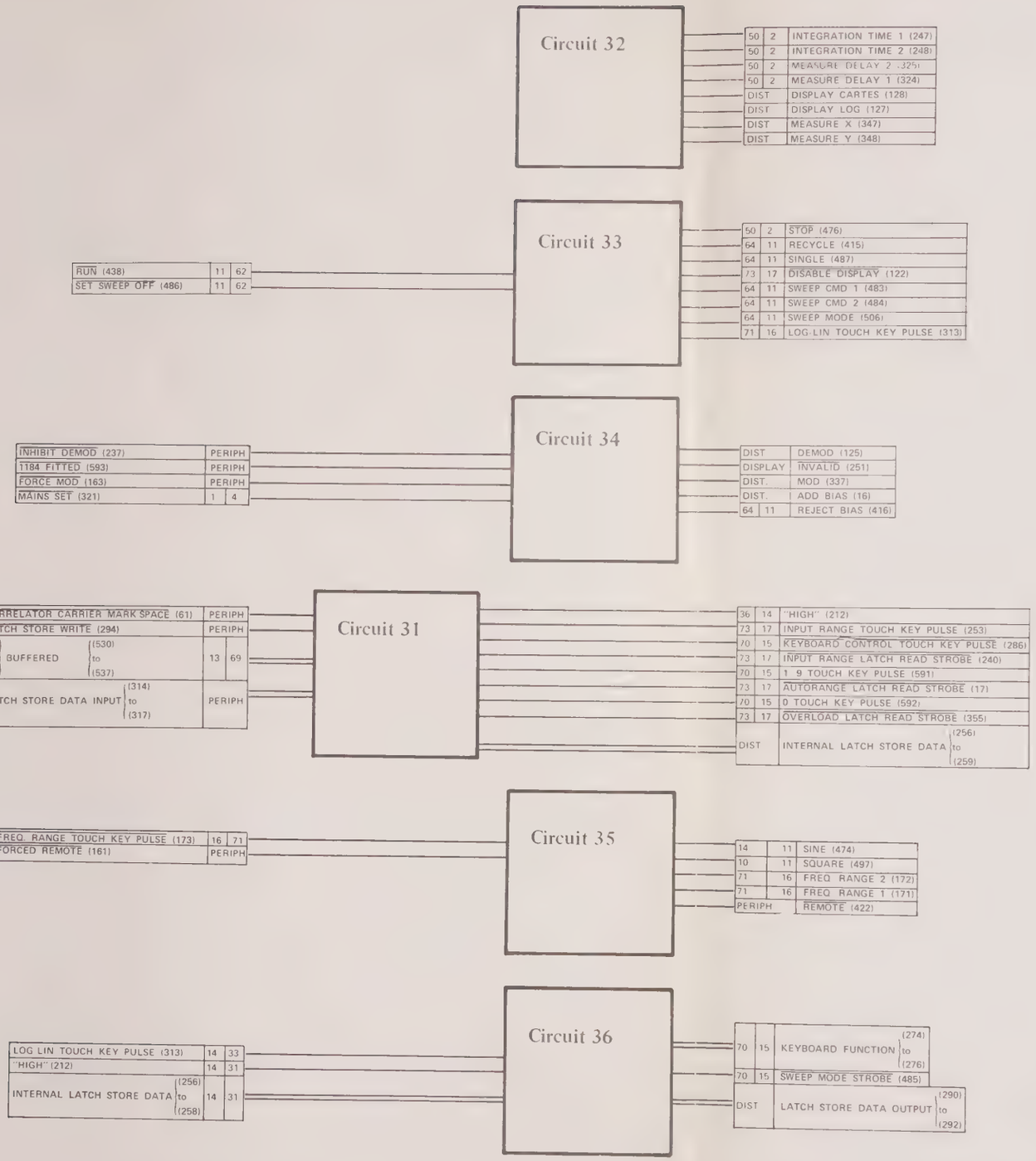

Circuit 32
50 2 INTEGRATION TIME 1 (247)
50 2 INTEGRATION TIME 2 (248)
50 2 MEASURE DELAY 2 (325)
50 2 MEASURE DELAY 1 (324)
DIST DISPLAY CARTES (128)
DIST DISPLAY LOG (127)
DIST MEASURE X (347)
DIST MEASURE Y (348)
Circuit 33
RUN (438) 11 62
SET SWEEP OFF (486) 11 62
50 2 STOP (476)
64 11 RECYCLE (415)
64 11 SINGLE (487)
73 17 DISABLE DISPLAY (122)
64 11 SWEEP CMD 1 (483)
64 11 SWEEP CMD 2 (484)
64 11 SWEEP MODE (506)
71 16 LOG-LIN TOUCH KEY PULSE (313)
Circuit 34
INHIBIT DEMOD (237) PERIPH
1184 FITTED (593) PERIPH
FORCE MOD (163) PERIPH
MAINS SET (321) 1 4
DIST DEMOD (125)
DISPLAY INVALID (251)
DIST. MOD (337)
DIST. ADD BIAS (16)
64 11 REJECT BIAS (416)
Circuit 31
CORRELATOR CARRIER MARK SPACE (61) PERIPH
LATCH STORE WRITE (294) PERIPH
T8 to T1 BUFFERED (530) to (537) 13 69
LATCH STORE DATA INPUT (314) to (317) PERIPH
36 14 "HIGH" (212)
73 17 INPUT RANGE TOUCH KEY PULSE (253)
70 15 KEYBOARD CONTROL TOUCH KEY PULSE (286)
73 17 INPUT RANGE LATCH READ STROBE (240)
70 15 1-9 TOUCH KEY PULSE (591)
73 17 AUTORANGE LATCH READ STROBE (17)
70 15 0 TOUCH KEY PULSE (592)
73 17 OVERLOAD LATCH READ STROBE (355)
DIST INTERNAL LATCH STORE DATA (256) to (259)
Circuit 35
FREQ. RANGE TOUCH KEY PULSE (173) 16 71
FORCED REMOTE (161) PERIPH
14 11 SINE (474)
10 11 SQUARE (497)
71 16 FREQ. RANGE 2 (172)
71 16 FREQ. RANGE 1 (171)
PERIPH REMOTE (422)
Circuit 36
LOG LIN TOUCH KEY PULSE (313) 14 33
"HIGH" (212) 14 31
INTERNAL LATCH STORE DATA (256) to (258) 14 31
70 15 KEYBOARD FUNCTION (274) to (276)
70 15 SWEEP MODE STROBE (485)
DIST LATCH STORE DATA OUTPUT (290) to (292)

Fig. 1.3.14

This diagram which is an extension of Fig. 1.3.13 shows the details of connections to circuits 31 to 36.

LATCH STORE CONTROL LINES

DIGITAL SECTION - MAIN STORE AND DISPLAY

This diagram should be examined in conjunction with that of the arithmetic unit. The main store, pcb 12, is common to the two diagrams and is the heart of the digital section.

Due to the complexity of interconnection and the type of signals involved, it is not normally possible to trace signal paths through this section. The paths shown must therefore be regarded as theoretical associations between circuits and not actual connections. The purpose of the diagram is to assist in locating a fault to the pcb involved rather than the faulty component.

OPERATION

The main store (pcb 12) contains all the numerical data used and displayed in the 1170. A complete list of these data is given in the instructions for the use of the Store State Indicator. (special test equipment type TG1212A).

Data are read from the store in many different ways but the general paths are shown on this diagram. Circuit No. 69, pcb 13 is used as an addressing system for the main store data, which is directed to the locations shown.

Part of this diagram is an extension of the Selector Latching diagram. The touch keys are shown connected to circuits 70 and 71. In fact this line represents keyboard data keyed in from the numerical touch buttons and is inserted via circuits 29, 30, 31 and 36. The data are held in the keyboard store until the ENTER key is touched, when they are entered into the MOS (main) store.

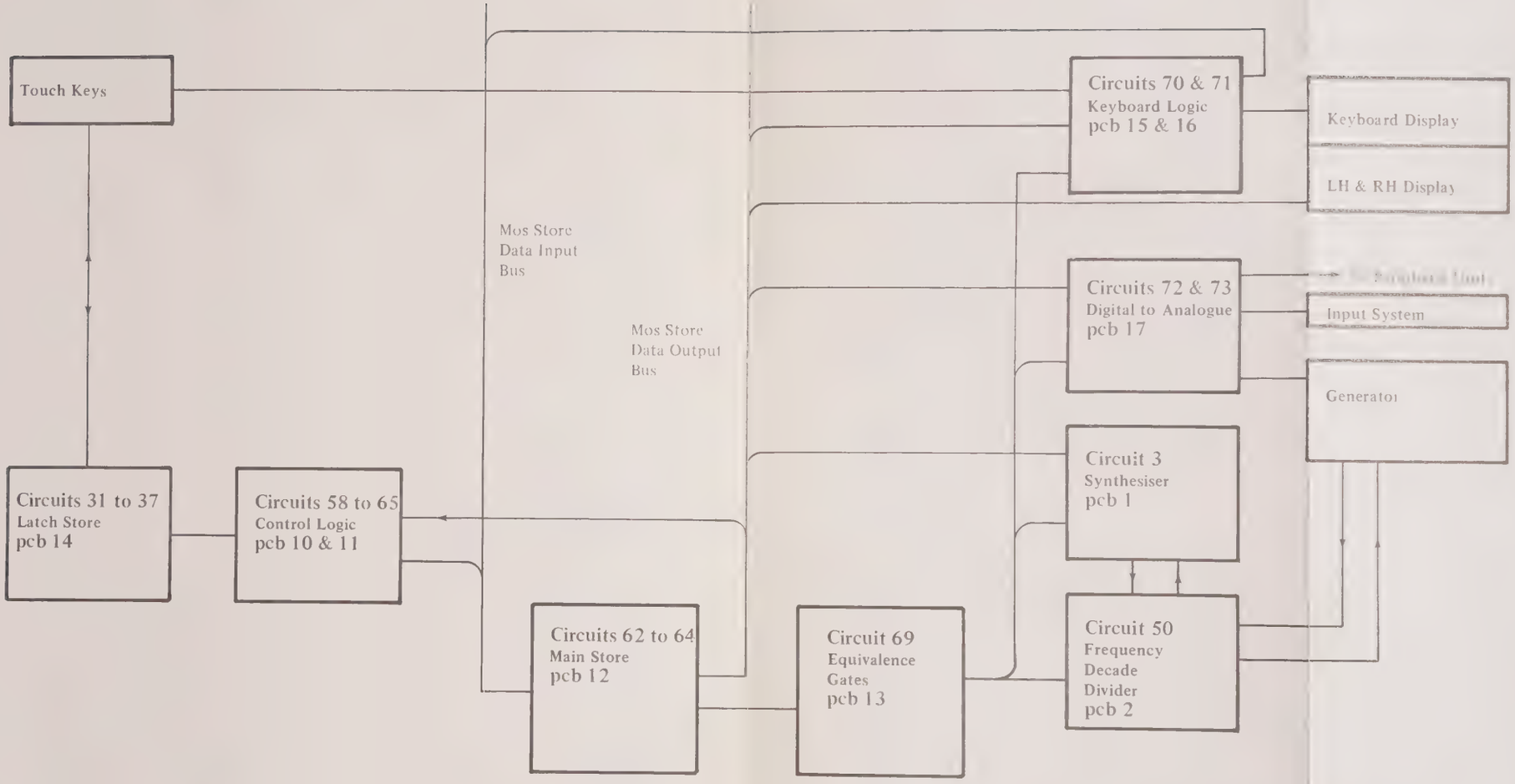


Fig. 1.3.15

DIGITAL SECTION, MAIN STORE AND DISPLAY

DIGITAL SYSTEM - ARITHMETIC UNIT

This diagram should be examined in conjunction with that of the Main Store and Display. Like that diagram this contains information regarding associations between circuit diagrams and pcb's and not actual connections between them.

A theoretical and mathematical description of this section is given from page 1.3.33.

As can be seen from this and its associated diagram, information is received from many sources into the arithmetic unit and, after processing, is deposited in the main store, for further processing or display.

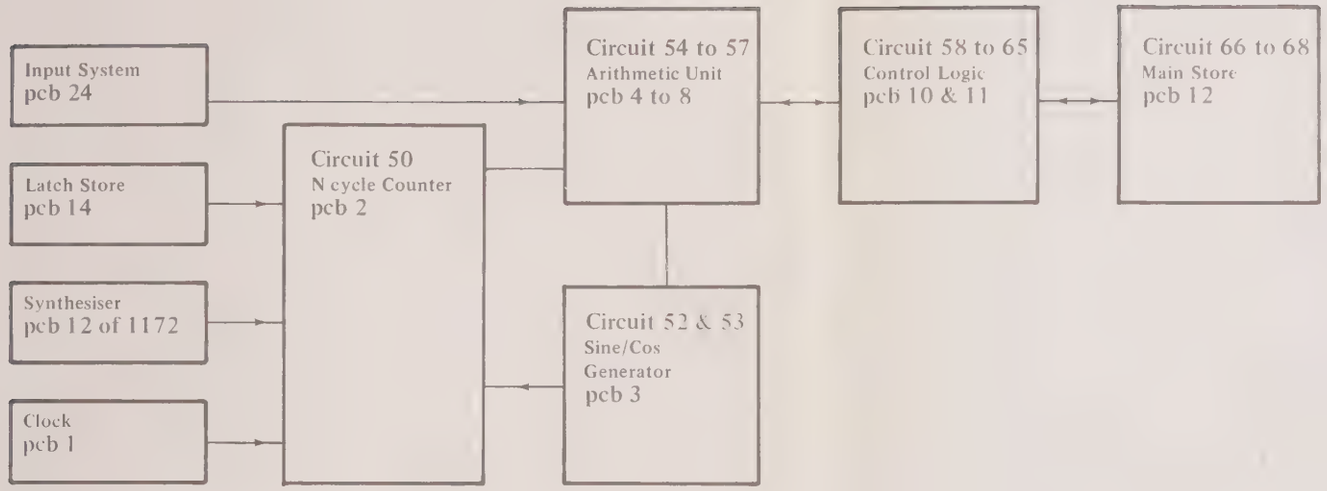


Fig. 1.3.16 DIGITAL SECTION - ARITHMETIC UNIT

CORRELATION IN THE 1170

INTRODUCTION

The 1170 is a "**Frequency Response Analyser**". It is usually used to measure the response of a system to a sine wave stimulating signal over a range of frequencies. Normally the stimulating signal is the output of the 1170 generator, a sine wave at frequency f.

The output of the system on test, can be split, by means of Fourier analysis, into a fundamental response (a sine wave at frequency f), harmonics (sine waves at integral multiples of frequency f) due to the non-linearities in the system on test together with any non-harmonically related noise. The 1170 measures the *fundamental* sine wave response, ignoring as far as possible any harmonics or random noise present. It is resolved into two components - one due to a sine wave IN-PHASE with the generator output, and one due to a sine wave in QUADRATURE with the generator output. This enables the PHASE response of the system to be measured, as well, as the AMPLITUDE response.

Measurements made over a range of frequencies enable the system frequency response, in phase and amplitude, to be built up.

BASIC PRINCIPLES

The 1170 uses a correlation process to measure the in-phase and quadrature components of the fundamental response of the system.

The generator output is a signal of the form $v_G = A_G \sin 2\pi ft$.

The output of the system on test is a signal $v_c(t)$..

To calculate the in-phase component at frequency f, this signal is multiplied by a signal $\sin 2\pi ft$, and integrated with respect to time, for a whole number of cycles N. This gives the result:

$$I_A = \int_0^T v_c\ (t)\ \sin 2\pi ft\ dt \qquad \text{where } T = \frac{N}{f}$$

Similarly the quadrature component is calculated by forming the integral,

$$I_B = \int_0^T v_c\ (t)\ \cos 2\pi ft\ dt$$

If the components of v_c (t) are A sin $2\pi ft$ (in-phase) and B cos $2\pi ft$ (quadrature) respectively, then:

$$I_A = \int_0^T (A \sin^2 2\pi ft + B \sin 2\pi ft \cos 2\pi ft)\ dt$$

$$= \tfrac{1}{2}A \int_0^T (1-\cos 4\pi ft)\ dt \quad + \tfrac{1}{2}B \int_0^T (\sin 4\pi ft)\ dt$$

$$= \tfrac{1}{2}AT - \tfrac{1}{2}A \int_0^T \cos 4\pi ft\ dt \quad + \tfrac{1}{2}B \int_0^T \sin 4\pi ft\ dt$$

For a whole number of cycles, the integrals in this expression are both zero, hence:

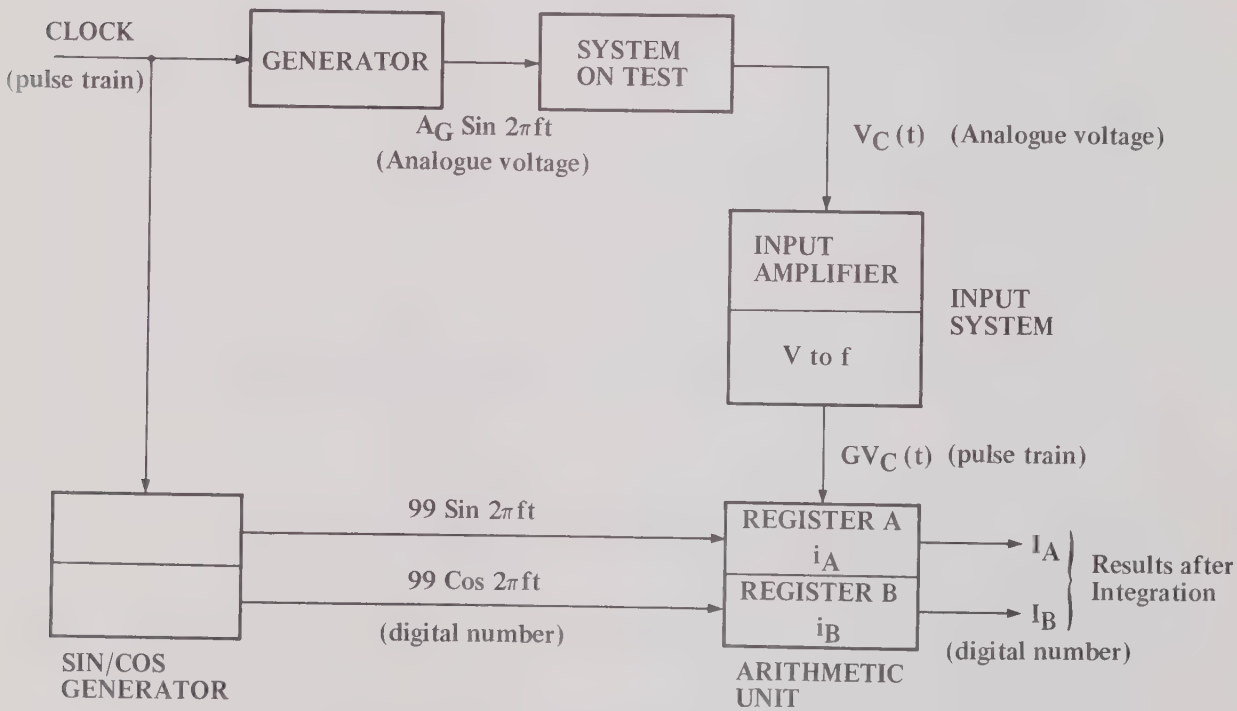
$I_A = \frac{1}{2}AT$. Similarly, $I_B = \frac{1}{2}BT$

Division by time of integration, T, allows the amplitudes of the in-phase and quadrature components, A and B, to be determined.

It can be shown that this method rejects harmonic components of $v_c(t)$ completely, and gives good rejection of random noise, which can be further improved by lengthening the integration time, T.

THE MECHANISM OF CORRELATION

The correlator contains a "sin/cos generator" (board 3), which produces the values of sin $2\pi ft$ and cos $2\pi ft$ necessary for the correlation process. The outputs of the sin/cos generator are two signed 2 digit BCD numbers, each in the range +99 to -99, equal to 99 sin $2\pi ft$ and 99 cos $2\pi ft$. The "sine" value is fed to arithmetic register A (board 5) and the "cosine" value to register B (board 6). These numbers are always available to the arithmetic unit, and follow the generator output sinewave.



CORRELATION IN THE 1170

The output of the system on test, $v_c(t)$ is applied to the correlator input terminals. It then enters the input system (boards 23 & 24), which consists of an input amplifier and a voltage to frequency converter (V to f), with an overall system gain of G pulses per second per volt.

The output of the V to f ($Gv_c(t)$ pulses per sec.) is fed to the arithmetic unit (board 4). On receiving each V to f pulse from the input system, the arithmetic unit adds the current value of "sine", presented to it by the sin/cos generator, to the contents of register A. Likewise, the current value of "cosine" is added to the contents of register B.

If the instantaneous contents of register A are i_A, and of register B are i_B, the rates of increase of the contents of the register are given by:

$$\frac{di}{dt}A = Gv_c\,(t)\,.99 \sin 2\pi ft \qquad \text{and} \qquad \frac{di}{dt}B = Gv_c\,(t)\,.99 \cos 2\pi ft$$

The final contents of the registers after the integration process are given by

$$I_A = \int_0^T Gv_c\,(t)\,.99 \sin 2\pi ft\, dt \qquad I_B = \int_0^T Gv_c\,(t)\,.99 \cos 2\pi ft\, dt$$

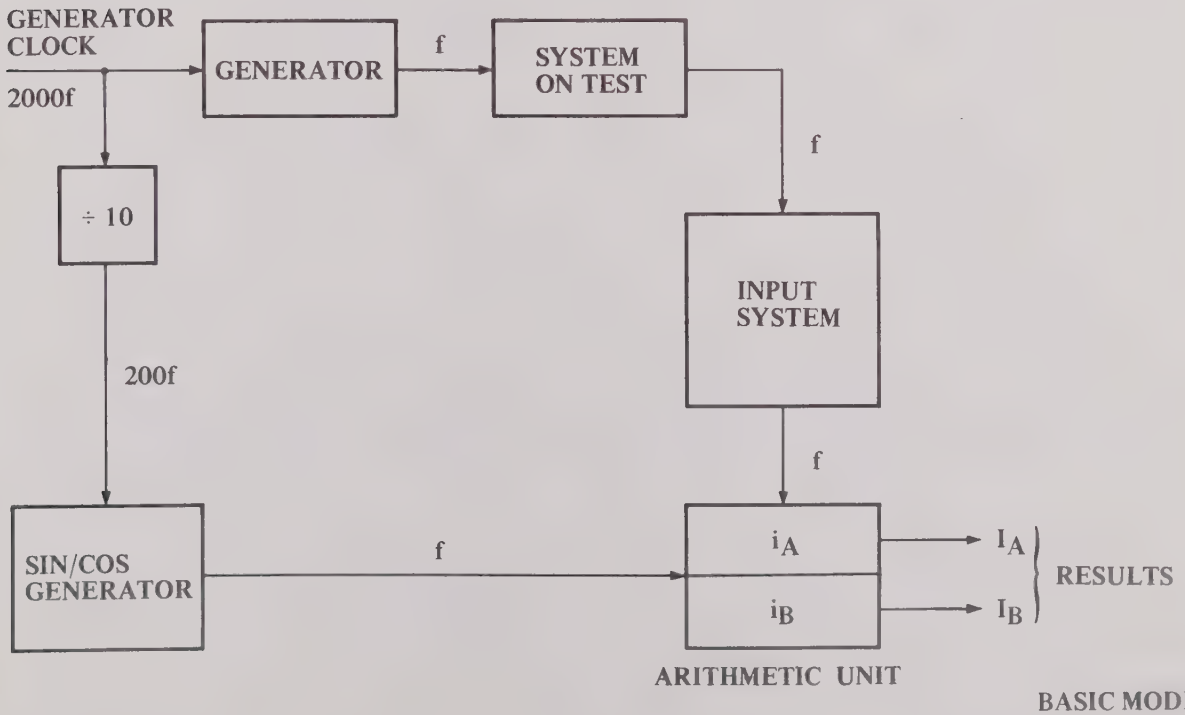
These results, with a suitable scaling factor, allow the in-phase and quadrature components of the system fundamental response to be calculated (see the explanation of the correlation process, above).

MODES OF OPERATION OF THE CORRELATOR

The sin/cos generator input to the arithmetic unit represents a sine wave at a certain frequency (the "correlator frequency"). The V to f signal is derived from the signal present on the analyser input terminals. The characteristics of the correlation process ensure that only the component of this V to f signal which is at the correlator frequency contributes to the result. If the correlator frequency is different from the frequency of the component of the input signal which is to be measured (the "measuring frequency"), the input system must change the frequency of the input signal before it reaches the V to f, so that the desired component will be correlated.

(a) Basic Mode

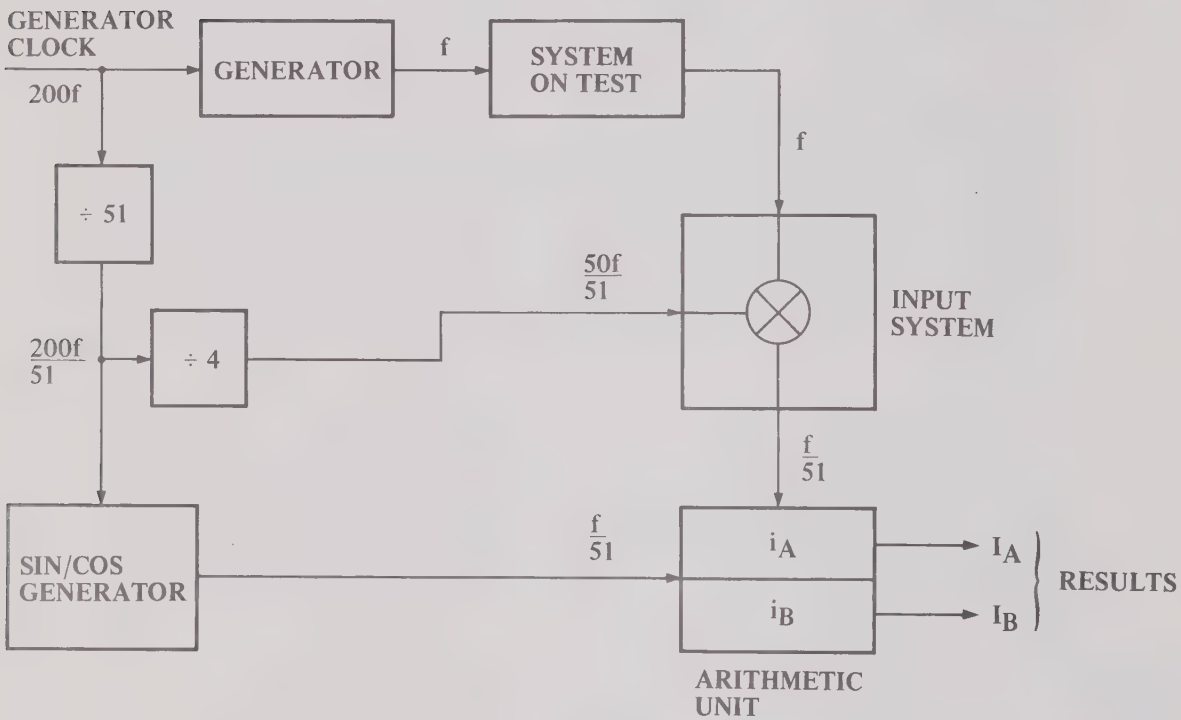
The basic mode of the correlator is used for measuring frequencies below 1kHz. In this mode, the correlator and the generator operate at the same frequency f. The frequency of the generator output sine wave is determined by the frequency of a clock signal (the "generator clock") which contains 2000 pulses for each cycle of output sine wave. The generator clock is thus at a frequency 2000f. This is divided by ten to produce the clock (200f) for the sin/cos generator, which always requires 200 pulses for each cycle. The sin/cos generator output thus represents a signal at frequency f, locked to the generator. The input system does not alter the frequency of the input signal, so the component at frequency f is measured.



BASIC MODE

(b) Heterodyne Mode

The correlator is capable of giving accurate results only up to a frequency of 1kHz. At measuring frequencies from 1kHz to 9.999kHz, the correlator operates at a lower frequency, enabling accuracy to be maintained. On this frequency range, the generator only requires 200 pulses per cycle. The generator clock is at frequency 200f. It is divided by 51 to produce the clock for the sin/cos generator (200f/51). The sin/cos clock is also divided by 4 to give a heterodyning signal at frequency 50f/51. The input system multiplies the input signal by this heterodyning signal, to produce a difference signal at the correlator frequency, f-50f/51=f/51.



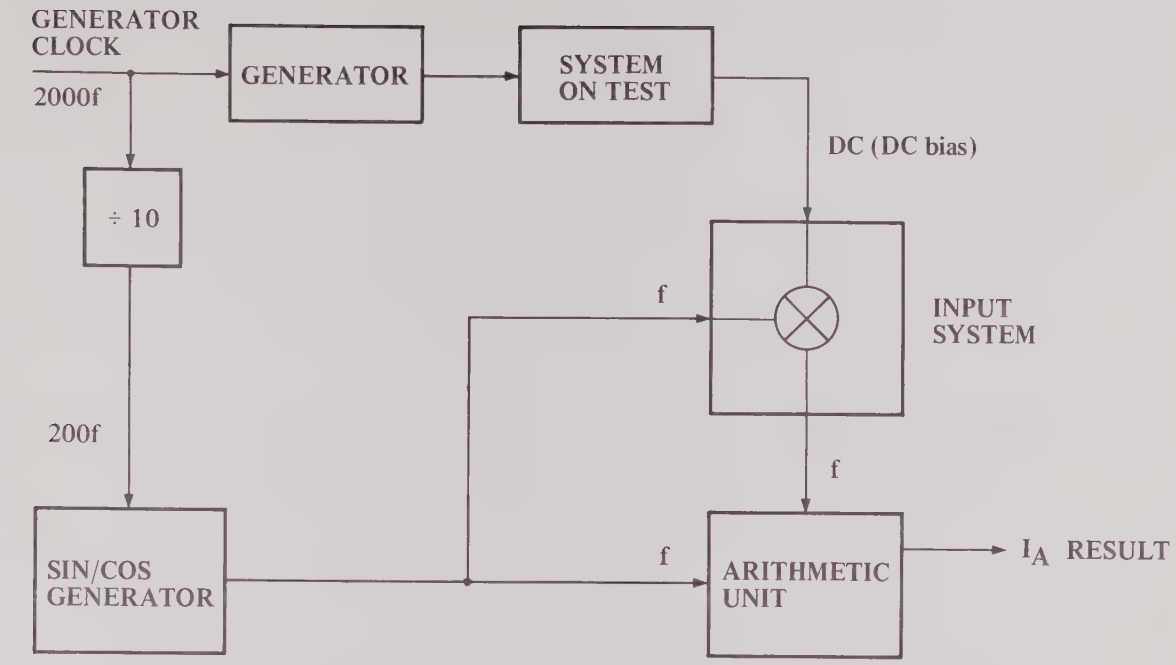
HETERODYNE MODE

(c) Measure Bias Mode

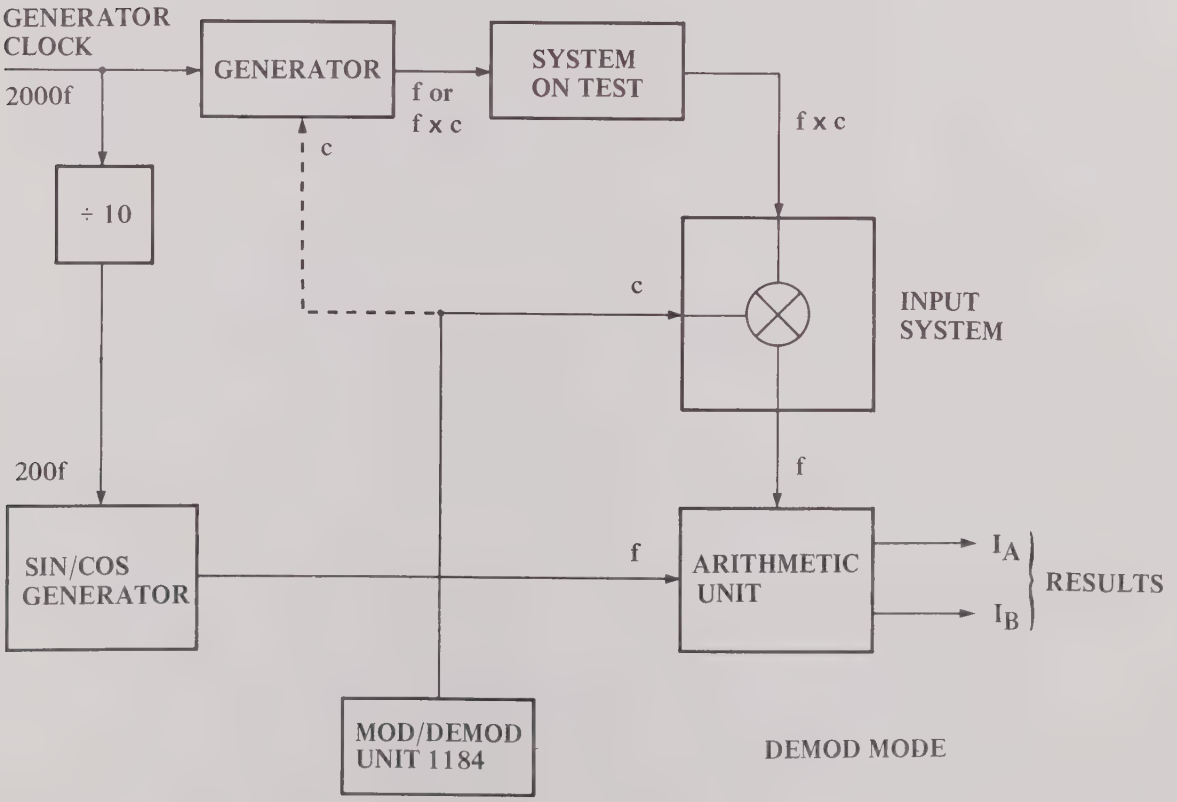
When "Reject Bias" is programmed, the correlator is used to measure the DC voltage on the input terminals, so that a "backing-off" voltage can be generated. This measurement is made in the "Measure bias" mode. The input to the correlator is multiplied by a square wave at the correlator frequency f. This converts any DC present to AC at frequency f, which is then correlated. (The "signal" present at the input terminal in converted to a mixture of DC and harmonics, all of which are rejected by the correlator, and thus does not interfere with the bias measurement).

(d) Demod Mode

When "Demod" is programmed, the output from the system under test is demodulated by multiplying it by a square wave at the carrier frequency c.



MEASURE BIAS MODE



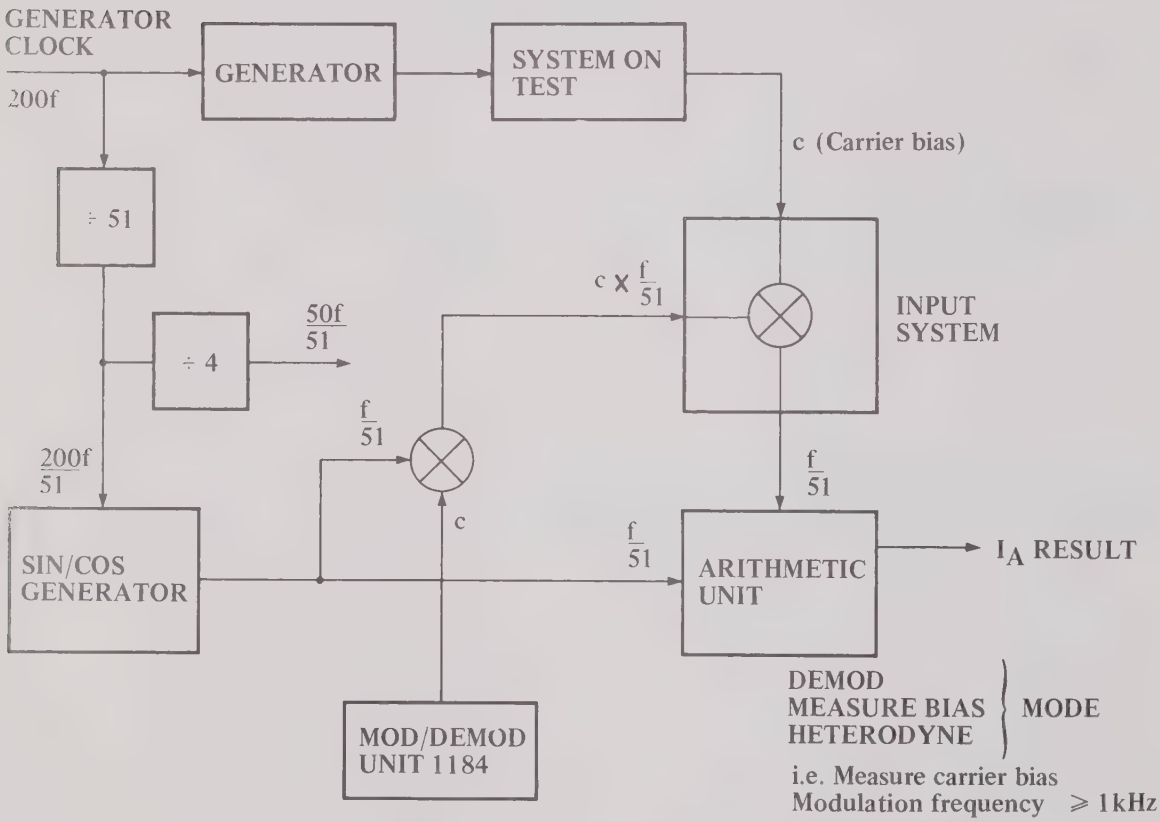
DEMOD MODE

(e) **Combinations of modes**

All combinations of modes are possible, viz

Measure bias	. Demod	i.e. measure carrier bias
*Measure bias	. Heterodyne	
Demod	. Heterodyne	i.e modulation freq$\geqslant$1kHz
*Demod	. Heterodyne . Measure bias	

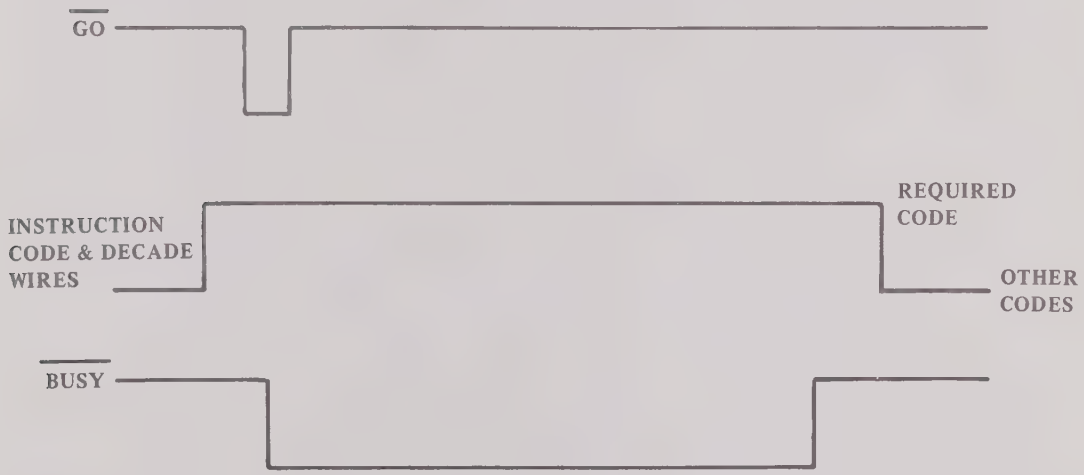
* In Measure bias mode, the output from the system under test is not multiplied by the heterodyning signal, as this is not necessary.



INTRODUCTION TO ARITHMETIC UNIT

The arithmetic unit is capable of performing 32 different operations. Some of these transfer information to or from the store. Some are simple calculations, such as an addition, and some are more complex, such as calculating the logarithm of a number. The most complex operation which can be performed autonomously by the arithmetic unit (in conjunction with the input system, the sin/cos generator and the N-cycle counter) is the correlation process itself (the operation performed by the arithmetic unit during the correlation process is termed "integration"). More complicated calculations are made up of sequences of instruction, which are commanded in turn by the control logic.

The control logic produces a 6 wire instruction code to the arithmetic unit. Five of these wires specify which of the 32 instructions the arithmetic unit is to perform. When the code has been set up, the control logic issues a $\overline{GO}$ pulse to the arithmetic unit, which is the command to start the specified operation. When the $\overline{GO}$ pulse has been accepted, the arithmetic unit returns a $\overline{BUSY}$ signal to the control logic. This inhibits further control logic action until the arithmetic unit operation is completed. The arithmetic unit then performs the operation. This may take 2μSec for a single addition, or several hours for a long integration. When it has finished it removes the $\overline{BUSY}$ signal to the control logic, which then continues to the next instruction in the program.



Arithmetic Unit Command Sequence

Some arithmetic unit operations make use of a decade number. This is produced by the control logic before the $\overline{GO}$ pulse, as a 3 wire binary number.

After an arithmetic unit operation, the control logic can use conditional instructions to sense various conditions in the arithmetic unit.

The arithmetic unit communicates data via a 4 wire static data bus. This allows it to transfer 4 bit numbers between registers within itself, or to and from the store. When communicating with the store, data is transferred between the arithmetic unit data bus (static) and the store data bus (dynamic i.e. changing every 2μSec) by an interface on Board 11, which is controlled by the control logic. Three "enables" wires, which are produced by the control logic, control which of the three registers in the arithmetic unit is allowed to write onto the data bus.

The signals described are sufficient for the arithmetic unit to perform any of its 32 operations except for integration (and measure delay), which is described later.

ARITHMETIC UNIT INTERNAL ORGANISATION

The arithmetic unit proper (excluding parts used only for integration and measure delay) consists of the following parts:

1. Decode Logic	Translates 5 instruction code wires from the control logic into the 22 wires necessary to control the individual parts of the arithmetic unit. (These wires are all static throughout an operation)
2. Condition Multiplexer	Used to feed information about the contents of the registers etc. to the control logic.
3. Sequence Logic	Receives the $\overline{GO}$ pulse from the control logic and generates all sequential pulses and clocks required by the various parts of the arithmetic unit. A $\overline{BUSY}$ signal is returned to the control logic to prevent it continuing to the next instruction until the current one has finished.
4. Registers A & B	Both registers are identical. Each stores a 9 digit BCD number, with sign, and is capable of adding or subtracting another 9 digit number from it, in 1.8μSec.
5. Register C	This is also referred to as the iteration counter or timer counter. It is a 6 digit BCD up/down counter. The i/p clock can be applied to any of its 6 stages, thus changing the significance of each i/p pulse.
6. Exponent Counters	Exp A and Exp B are 4 bit counters, used to keep the exponents of the contents of register A and B during shift operation etc. They can be read by, or loaded from the store, via the data bus. An Exp C is also available and can be read by the store (it cannot be loaded). It is always equal to Exp B - Exp A.

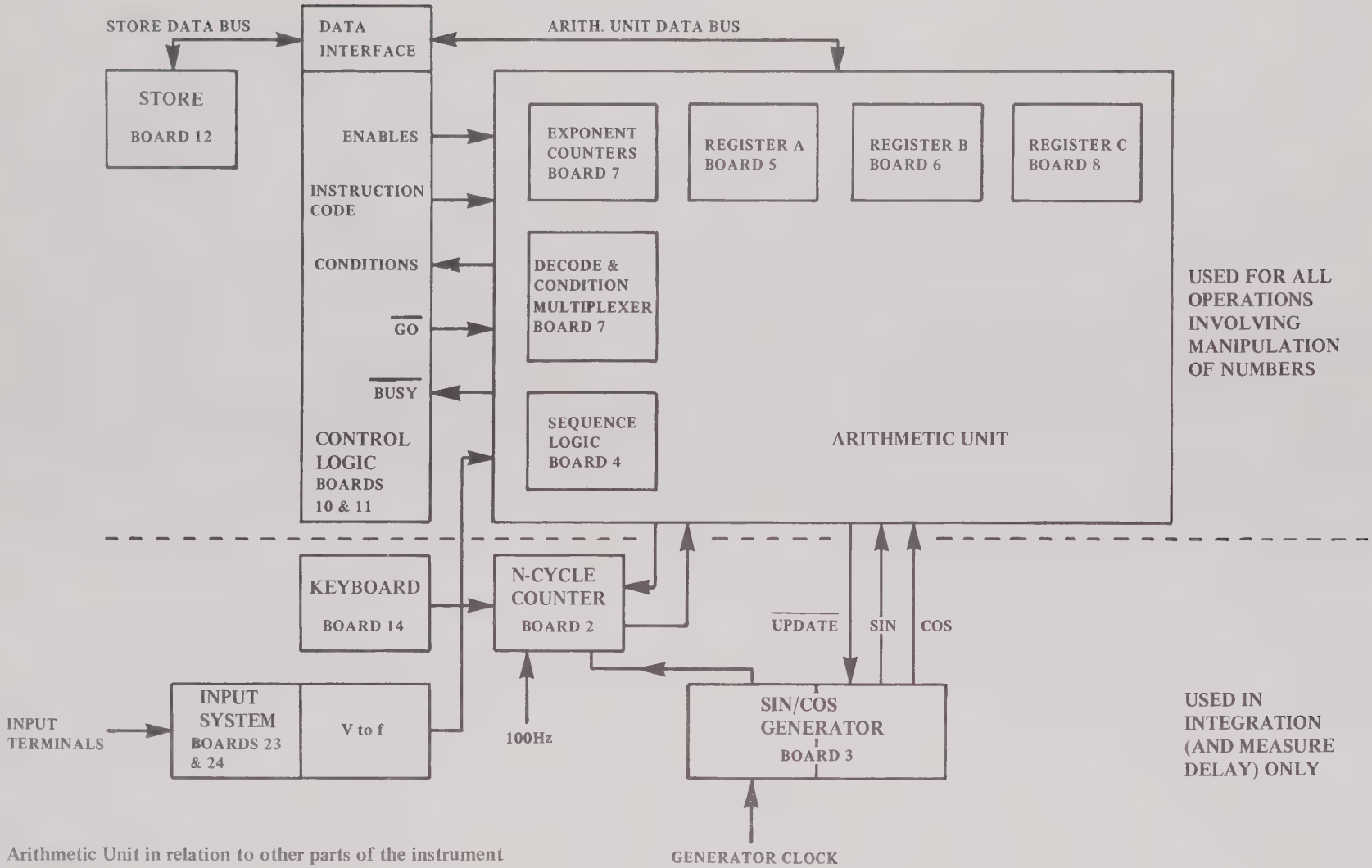
The arithmetic unit operates in "cycles". Each cycle takes 1.8μSec. Some arithmetic unit operations take only one cycle (e.g. an addition or a transfer of one digit between a register and the data bus), others may take up to 2 or 3 thousand cycles (e.g. calculating a logarithm) whilst integration may take a more or less unlimited number of cycles.

Registers A and B can each store a 9 digit BCD number, and a sign, indefinitely. The most significant digit is an overflow digit, and is known as the 9th digit. The remaining digits are numbered from 0 (most significant, except for the 9th digit) to 7 (least significant). In a single cycle, either or both registers can add or subtract another 9 digit number (the "input data") from the current contents of the register. The answer becomes the new contents. More complex operations are made up of many such cycles, each consisting only of additions or subtractions. Each register can select one of a number of sources from which the input data may come. Each register produces 3 output signals which may be used as input data either by itself or by the other register. The outputs are equal to:

(a)	the register contents	A	B
(b)	the register contents x10	10A	10B
(c)	the register contents ÷ 1000	A/1000	B/1000

Input data may also come from other sources (data bus, sin/cos generator, or log constant from board 4). The registers may add none, some or all of the 9 digits of the input data. The number may be added to the current register contents, or the current contents may be discarded and the input data added to zero. Different combinations of these alternatives produce all possible types of cycle which the arithmetic unit can perform.

The various cycle types are described in Table A.



Arithmetic Unit in relation to other parts of the instrument

SEE NOTE NO.	DIGITS OF INPUT DATA ADDED 9th 0 1 2 3 4 5 6 7	REGISTER A: ADD/SUB	REGISTER A: SOURCE OF I/P DATA	REGISTER B: ADDED TO	REGISTER B: ADD/SUB	REGISTER B: SOURCE OF I/P DATA	DECADE NO.	INSTRUCTION NAME	CODE	NOTES
[illegible]			Zero	Current conts.		Zero		Read	12	Also used for CLoad, AExp dec, BExp dec
2			Zero	Zero	+	Register B		AClear	8	
[illegible]		+	Register A	Zero		Zero		BClear	9	
[illegible]			Zero	Current conts.	+	Register A		BAdd	0	
[illegible]			Zero	Current conts.	-	Register A		BSub	1	
[illegible]		+	Register B	Current conts.		Zero		AAdd	2	
[illegible]		-	Register B	Current conts.		Zero		ASub	3	
[illegible]		+	Register A	Current conts.		Zero		ADouble	19	
[illegible]			Zero	Current conts.	+	Register B		BDouble	20	
[illegible]		+	Register B	Zero	+	Register A		Swap	21	
[illegible]		-	Register A	Zero	+	Register B		AInv	17	Subtracts Register A from zero, forming 10s complement
7			Register A	Zero		Register B		Complement	18	Subtracts either register from zero if it is negative
[illegible]		+	10A	Zero	+	Register B		ATen	29	Shifts register A one decade up
[illegible]		+	Register A	Zero	+	10B		BTen	30	Also used for CTen. Shifts register B one decade up
[illegible]		-	10A	Current conts.		Zero		Ax-9	16	Multiplies register A by -9
[illegible]		+	Data bus	Current conts.		Zero	0	ALoad	10	Also used for AOne load
							1			
							2			
							3			
							4			
							5			
10			Zero	Current conts.	+	Data bus	0	BLoad	11	Also used for BOne load
							1			
							2			
							3			
							4			
							5			
[illegible]		-	Log const.	Current conts.	+	B/1000		Log	4	
[illegible]		+	Log const.	Current conts.	-	B/1000		Exp	5	
[illegible]		+	B/1000	Current conts.	-	A/1000		Polar	6	
[illegible]		-	B/1000	Current conts.	+	A/1000		Cartes	7	
[illegible]			Zero	Current conts.	-	Register A		XDivide	22	} Iterative operations (10 cycles max) used in the division routine.
[illegible]			Zero	Current conts.	+	Register A		YDivide	23	
[illegible]			Zero	Current conts. ÷ 10		Zero		DTen	26	Shifts both registers one decade down.
[illegible]			Sin "1" digit	Current conts.		Cos "1" digit		} Int	24	
[illegible]			Sin "10" digit	Current conts.		Cos "10" digit				

The ADDED TO column refers to **both** registers. The contents of register A after an operation is the sum (or difference) of the SOURCE OF INPUT DATA (Reg A) column and the ADDED TO column. Thus for AAdd, the contents of register A after the operation is Register B + Current conts of Register A. Similarly for register B.

The DIGITS OF INPUT DATA ADDED column shows which digits of the input data are added to (or subtracted from) the register. Thus the data bus is added to one digit only, in a Load operation, and the least significant 6 digits only of the B/1000 signal are used in a Log operation.

NOTES

SINGLE CYCLE OPERATIONS

1. Registers A & B are each equipped with an "output latch", which is used when a digit is read from the register onto the data bus. Digits 0 to 5 may be read onto the bus. If one of these is selected by the "decade" wires (from the control logic), it is entered into the output latch during any cycle performed by the arithmetic unit, of whatever type. The contents of the latch are read onto the data bus when the "enable" wire (from the control logic) for the register is high. Normally the sequence to read a digit consists of setting up the decade wires to the desired digit number, performing a "read" operation in the arithmetic unit, and enabling the register which is to be read. The desired digit is then present on the data bus and may subsequently be loaded into another register, or the store.

The "read" operation does not alter the contents of either register. Its function is to ensure that the desired digits are entered into the output latches.

It is also used for certain auxiliary operations which affect only the exponent counters or register C. Signs and exponents, and data in register C, are read onto the data bus immediately their decade number and enable wire are set up (i.e. they do not require a cycle to "latch" them). However, for the sake of uniformity, a "read" operation is normally performed as for digits 0 to 5 of registers A and B.

For the purpose of communication via the data bus the signs are allocated decade number 6 (+ve = value 0, -ve = value 1) and exponents decade number 7.

2. **Clear** operations clear all 9 digits of the register in question to zero. The signs and exponents are unaffected by a clear operation. In order to clear them it is necessary to load zero into them from the data bus. This is also true of register C (there is no CClear operation).

3. **Additions and subtractions** are single cycle operations. They are full 9 digit calculations. Carries and borrows out of the 9th decade are lost. The sign bistables will follow changes of sign correctly only if negative numbers are in 10's complement form before the addition or subtraction. Answers will then also be in 10's complement form if negative. If the signs are not of interest, additions and subtractions may be performed on numbers in "absolute value and sign" form - the operation will take place on the absolute values, the result will be complemented if the difference in absolute values (in a subtraction) was negative, and the signs will not have any straightforward meaning after the operation.

4. **"Double"** operations are performed by adding the number to itself. Signs are unaffected, and carries out of the 9th decade are lost.

5. A **"Swap"** operation adds the contents of register A to register B, and the contents of register B to register A. The input data is added to zero in each register. Signs and exponents are unaffected (i.e. they are NOT swapped).

6. An **"AInvert"** operation subtracts the contents of register A from zero. Register B and both signs are unaffected.

7. **Complement**. The register are set up as if they were each to subtract their current contents from zero. However, gates on boards 5 and 6 ensure that they are subtracted if negative, and added if positive. The 10's complement is thus formed. Signs are unaffected. This operation is used to convert numbers in "absolute value and sign" form to 10's complement form and vice versa.

8. **ATen, BTen, and CTen** operations add the current contents x10 to zero in one register, the the contents of which are thus shifted up one decade, and add the contents to zero in other register, which is thus unaffected. The 10A and 10B signals are formed by a circulair shift process, so that the 9th decade of the contents of register A becomes digit 7 (least significant digit) of signal 10A. Signs are unaffected by the operation. In ATen and BTen operations, the exponent of the register being shifted is reduced by one, to keep the magnitude represented by the register constant. Exponents are not affected by CTen (this is the only difference between BTen and CTen).

9. The **Ax-9** operation subtracts 10A from A, giving a result -9A. In conjunction with AInvert, this enables numbers to be multiplied by 9, which is useful in calculating degrees from radians. Register B, signs and exponents are unaffected by the operation.

10. **ALoad and BLoad.** These operations add the data present on the data bus to the register, in one digit position only between 0 and 5. It is not necessary for the register to contain zero before the operation - input will be added correctly (loading of register A and B is additive). If digits 6 (sign) or 7 (exponent) are addressed, the contents of the register will remain unchanged, but the data present on the data bus will replace the current contents of the sign bistable or the exponent counter of the register in question (loading of signs and exponents is destructive). The 9th digit 6 and7 of the registers themselves cannot be loaded from or read onto the data bus.

11. **CLoad.** One of digits 0 to 5 of register C may be loaded from the data bus by a CLoad operation. This is accompanied by a "read" operation which has no effect on the contents of register A and B. Loading of results C is *destructive* - no CClear operation is provided. If digit 6 or 7 is addressed, the CLoad operation has no effect at all.

ITERATIVE OPERATIONS

Outputs are provided from registers A and B to show when a carry or borrow from digit 0 into the 9th decade has occurred. An output is provided from register C to show when it has counted to state zero, either by overflowing (when counting UP) or by counting DOWN to zero. Circuitry is provided (Board 4) so that when commanded to "go" by the control logic, the arithmetic unit will perform cycles continuously until one of the above three things happens. The arithmetic unit then returns control to the control logic by removing the $\overline{\text{BUSY}}$ signal. Counting to zero in register C will always terminate an iterative operation. Some iterative operations are also terminated by a carry or borrow in either register A or register B.

12. **Log.** In a cycle of a "log" operation, B/1000 is added to the current contents of register B. This has the effect of multiplying the contents of register B by 1.001. A constant (log const.) equal to log 1.001 (= .00043402) generated on board 4, is subtracted from register A.

Since the B/1000 signal is generated by a circular shift process, the least significant three digits of B appear as the most significant 3 digits of B/1000, which should all be zero. Therefore in operations involving the B/1000 and A/1000 signals, only the least significant 6 digits of the input data are added to the registers.

The log operation commences with the number whose log is to be found in register B. Its most significant digit must be in digit 0 position (i.e. the number must be "normalised"). Register A contains zero, or a digit in the 9th decade only. Cycles of the type described above are then executed continuously until the signal indicating a carry into the 9th decade of register B appears. When this is received by the sequence logic (Board 4) it terminates the operation and removes the $\overline{\text{BUSY}}$ signal to the control logic, which continues to the next instruction in the program.

If we treat the decimal point of the registers as being between the 9th decade (integer part) and the rest of the register (fractional part), then the function of the log operation is to determine how many times it is necessary to multiply the initial value B ($1 > B \geqslant .1$) by 1.001 in order to make it $\geqslant 1$. This number is equal to the number of cycles performed, N.

This gives:

$$1 \approx B \times 1.001^{N}$$

taking logs: $0 = N \log 1.001 + \log B$

Simultaneously, the number $-N \log_{10} 1.001$ is calculated in register A, by subtracting the log constant, .00043402 (= log 1.001) from it once for each cycle performed.

Therefore:

A (final value of register A) $\approx$ - N $\log_{10}$ 1.001

substituting for N log 1.001 from above : $A \approx \log_{10} B$

Signs and exponents are not affected by this operation. Register C counts the number of cycles performed. This used as a safety measure to ensure that the operation will stop after 10000 cycles if an attempt is made to find the log of zero.

13. **Exp.** This operation is used to calculate antilogs. The operation starts with the number whose antilog is to be found in register A, and 1.0 in register B. The process is exactly the same as the log process, except that the log constant is *added* to register A, and the signal B/1000 *subtracted* from register B each cycle. The iteration continues until there is a carry into the 9th decade of *register A.*

This is equivalent to the calculation:

$$N = \frac{-A}{\log(1.001)}$$

$$B = 1.0 \times (.999)^N$$

hence: $N \log(1.001) = -A$

$N \log_{10} .999 \approx A$ since log 1.001 $\approx$ -log .999

taking antilogs: $(.999)^N \approx 10^A$

$B \approx 10^A$ (i.e. antilog A)

where A = initial value of register A
B = final value of register B
N = number of cycles performed

Signs, exponents and the contents of register C are not affected by this operation. It cannot continue for longer than 1/.00043402 (= 2305) cycles, regardless of the initial contents of the registers.

14. **Polar.** In a cycle of the "polar" operation, the B/1000 signal is added to register A, and the A/1000 signal subtracted from register B. The operation continues until a borrow from the 9th decade of B occurs (i.e. register B becomes negative). The number of cycles performed is counted by the iteration counter (register C). At the beginning of this operation, register A contains the "in-phase" component of the result of the measurement, register B the "quadrature" component, and the iteration counter contains zero. Each cycle is equivalent to rotating the vector represented by A and B towards the real axis by an angle of .001 Radians. This continues until the "quadrature" component becomes zero. At this point, the real part of the vector (the contents of register A) is equal to its amplitude, R, and the angle through which it has been rotated (i.e. the contents of the iteration counter) is equal to its phase angle, θ. Signs and exponents are not affected by this operation.

As for "Log", the operation will be terminated by the iteration counter after 10000 cycles if an attempt is made to convert a zero vector to polar form. The maximum number of cycles which can legitimately occur (corresponding to a rotation of 90^o) is $1000\pi/2$ (= 1571).

15. **Cartesian.** This operation is the reverse of "polar". Cycles are the same as cycles of the polar operation except that the B/1000 signal is *subtracted* from register A, the A/1000 signal is *added* to register B, the iteration counter counts *down* one for each cycle, and iterations continue until the iteration counter reaches zero. The operation starts with the vector amplitude (R) in register A, zero in register B, and the phase angle (θ), in milliradians, in the iteration counter. The operation consists of rotating the vector away from the real axis, in 1 milliradian steps, through an angle θ. Registers A and B are then equal to the "in-phase" and "quadrature" components of the vector.

A borrow occurring in register A will also terminate the "Cartesian" operation. This is a safety measure, as if register A became negative it would be in complement form, which could cause large errors in register B if the process were allowed to continue. The characteristics of this process are such that register A can become negative slightly before the vector has been rotated through 90° (the maximum allowed). Signs and exponents are not affected by this operaton.

16. **XDivide, YDivide.** These operations are used in the division routine. In the XDivide operation, the contents of register A are subtracted from the contents of register B repeatedly until register B become negative. The number of cycles performed is counted in the addressed decade of the iteration counter. The division routine is arranged so that the contents of register B are always less than 10 times the contents of register A before the XDivide operation. The maximum number of iterations performed is thus 10. The YDivide operation is exactly the same, except that register A is *added* to register B until it becomes *positive,* and the iteration counter counts *down* instead of up.
Signs and exponents are not affected by these operations.
For a more complete description of the division routine, see "THE 1170 SOFTWARE".

17. **Decsh.** Within each of registers A and B, it is possible to perform a circular shift of the digits, so that the contents of the registers are divided by ten. Since this circular shift operation would result in the least significant digit of the old register contents becoming the most significant digit of the new contents, this digit is gated out so that it is always zero after a Decsh operation. This is accomplished internally by the registers when commanded to operate in DECSH mode. Signs are not affected by the operation, and the exponents are both increased by one, to keep the magnitudes of the numbers being represented by the registers constant.

18. **Integrate.** In a single cycle of the integrate operation, the least significant digit (the "1" digit) of the "sine" signal, from the sin/cos generator, is added to or subtracted from the least significant digit of register A, and the least significant digit of the "cosine" signal added to or subtracted from the least significant digit of register B. Then (within the same cycle) the source of the input data is changed to the most significant digits (the "10" digits) of the "sine" and "cosine" signals, and these are added to or subtracted from the next digit in the registers (digit no. 6). Carries or borrows into the remaining 7 digits of the registers can occur, but no data is added.

Exponents are not affected by the "integrate" operation, but the signs follow the signs of the registers. These may change many times during a complete integration.

INTRODUCTION TO BOARD 3

The circuitry housed on board 3 can conveniently be divided into 4 sections as follows:

SIN/COS GENERATOR
DIVIDE BY 10/51 COUNTER
SET 0^{o} LOGIC
CHOP SIGNAL GENERATOR

These sections are used only during the integration section of each measurement sequence.

SIN/COS GENERATOR

This section receives a clock (SIN/COS CLOCK) from the divide by 10/51 counter. This clock has 200 pulses per correlator cycle. In response, the sin/cos generator produces two signed 2 digit BCD numbers representing sin $2\pi ft$ and cos $2\pi ft$, which are fed to arithmetic registers A and B respectively (boards 5 & 6).

DIVIDE BY 10/51 COUNTER

The divide by 10/51 counter has as its input the generator clock and produces as its output the sin/cos clock.

At frequencies below 1kHz, the correlator and generator run at the same frequency, f. The generator clock (2000f) is divided by 10 to produce the sin/cos clock at frequency 200f.

At frequencies $\geqslant$1kHz, the correlator operates in the "heterodyne" mode. The generator clock (200f) is divided by 51 to produce the sin/cos clock at frequency 200f/51. A further divide by 4 counter produces the heterodyning signal (50f/51).

The sin/cos clock is wire-OR-able, enabling the correlator frequency to be modified. This is used in particular by the 1185 Harmonic Analysis option, which adds clock pulses to the sin/cos clock, causing the correlator to run at a multiple of its fundamental frequency.

The basic sin/cos clock (before wire-OR-ing) is fed to the n-cycle counter (renamed N-CYCLE CLOCK), so that integration is always for a whole number of cycles of the correlator *fundamental* frequency.

SET 0^{o} LOGIC

The correlator must be set to 0^{o} whenever one of the following two cases apply.

(a) when the generator passes through 0^{o} (or $\geqslant$1kHz, every 51 times the generator passes through 0^{o}) and,

(b) when the external world sets the generator to 0^{o}.

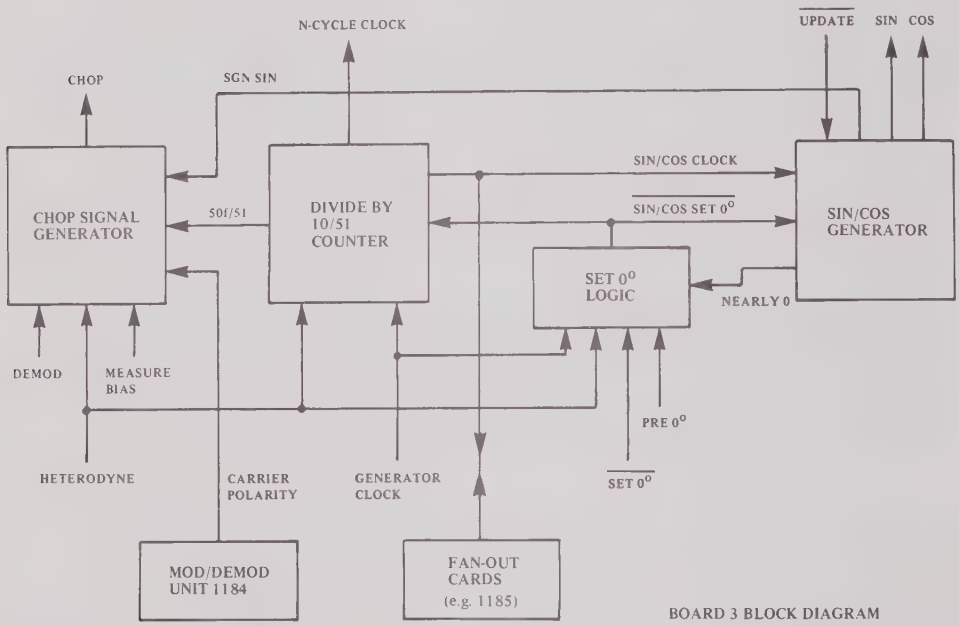
Case (a) is indicated by the PRE 0^{o} signal and case (b) by the $\overline{\text{SET } 0^{o}}$ signal. The SET 0^{o} logic combines these two signals, disables 50 out of 51 0^{o} pulses if f $\geqslant$1kHz, and produces a signal $\overline{(\text{SIN/COS SET } 0^{o})}$ to set the sin/cos generator and the divide by 10/51 counter to the 0^{o} state.

CHOP SIGNAL GENERATOR

The input system requires a square wave signal (CHOP) by which to multiply the input signal when not in its basic mode. When the machine is heterodyning the 50f/51 signal is used; when demodulating, the carrier polarity signal (CARRIER POS) is used and when measuring bias the correlator polarity signal (SGN SIN) is used.

The machine can be doing more than one of these things at once (e.g. measuring carrier bias, in which case both the DEMOD and MEAS BIAS modes are used, or demodulating above 1kHz where DEMOD and HETERODYNE modes are used).

The chop signal generator selects and combines the required signals, stretches any resulting pulses which are too short for transmission through a pulse tranformer, and feeds the signal (CHOP) to the input system.



BOARD 3 BLOCK DIAGRAM

INTRODUCTION TO BOARD 8

Board 8 houses "Register C", also known as the "iteration counter" or "timer counter". Its function is to count the cycles performed in an iterative operation (LOG, POLAR, CARTES, or a step in the division routine, XDIVIDE, YDIVIDE), and to measure the time taken by the integration operation.

It consists of the following functional blocks:-

COUNTER

This is a 6 digit, synchronous, up/down counter (IC7 to 12, plus associated gates). The mode of the counter (UP or DOWN) is controlled by a wire from the Decode logic (board 7). The counter is arranged so that the clock may be applied to any of its 6 digits, thus altering the "significance" of the clock. This is controlled by the three decade wires.

DECADE No.	CLOCK SIGNIFICANCE
0	100,000 bits
1	10,000 bits
2	1,000 bits
3	100 bits
4	10 bits
5	1 bit
6 or 7	0 (no count)

Digits less significant than the addressed digit are not affected by the clock. Carries or borrows into digits more significant than the addressed digit occur normally.

Example Decade No. = 3
UP/DOWN = UP

Initial contents	005741
After 1 clock pulse	005841
2	005941
3	006041
4	006141
	etc.

Any one of the 6 digits of the counter may be loaded from the data bus. If the LOAD C wire (from Decode logic) is high, a pulse on the ITERATION CLOCK wire, which occurs once for each cycle performed by the arithmetic unit, will cause the digit on the data bus to replace the addressed digit in the counter. The old digit is lost. Unaddressed digits are not affected by a load operation. If the decade number is 6 or 7, none of the digits are affected. A CLoad operation (see Decode logic truth table) consists of a "read" cycle, which does not affect the contents of registers A or B, performed with the LOAD C wire high.

DATA OUTPUT MULTIPLEXER

Any one of the 6 digits of the counter may be read onto the data bus. The multiplexer section receives the data from each of the 6 digits, selects the output from the addressed digit (if the decade number is between 0 and 5) and reads it onto the data bus if the ENABLE C line (from the control logic) is high. The multiplexer section consists of 6 sets of 4 gates (IC1 to 6) which are wire-OR-ed together, a set of "enable" gates (IC22) and a set of 4 drivers for the data bus (IC24).

CLOCK CONTROL

This section consists of IC27a and IC25c.

During single cycle operations, the iteration counter is not affected. In this case the ITERATE wire and the INTEGRATE wire (from Decode logic) are both low, and the counter receives no clock.

During iterative operations, the counter is required to count the number of cycles performed. In this case the ITERATIVE wire is high, and the counter counts the number of pulses on the ITERATION CLOCK wire, which is equal to the number of cycles performed by the arithmetic unit.

During integration, the counter is required to measure the time of integration. The INT wire is high, and the ITERATE and the $\overline{\text{BUSY}}$ wires low. The counter thus counts $\overline{\text{TIMER CLOCK}}$ signal (see "CONTROL OF INTEGRATION").

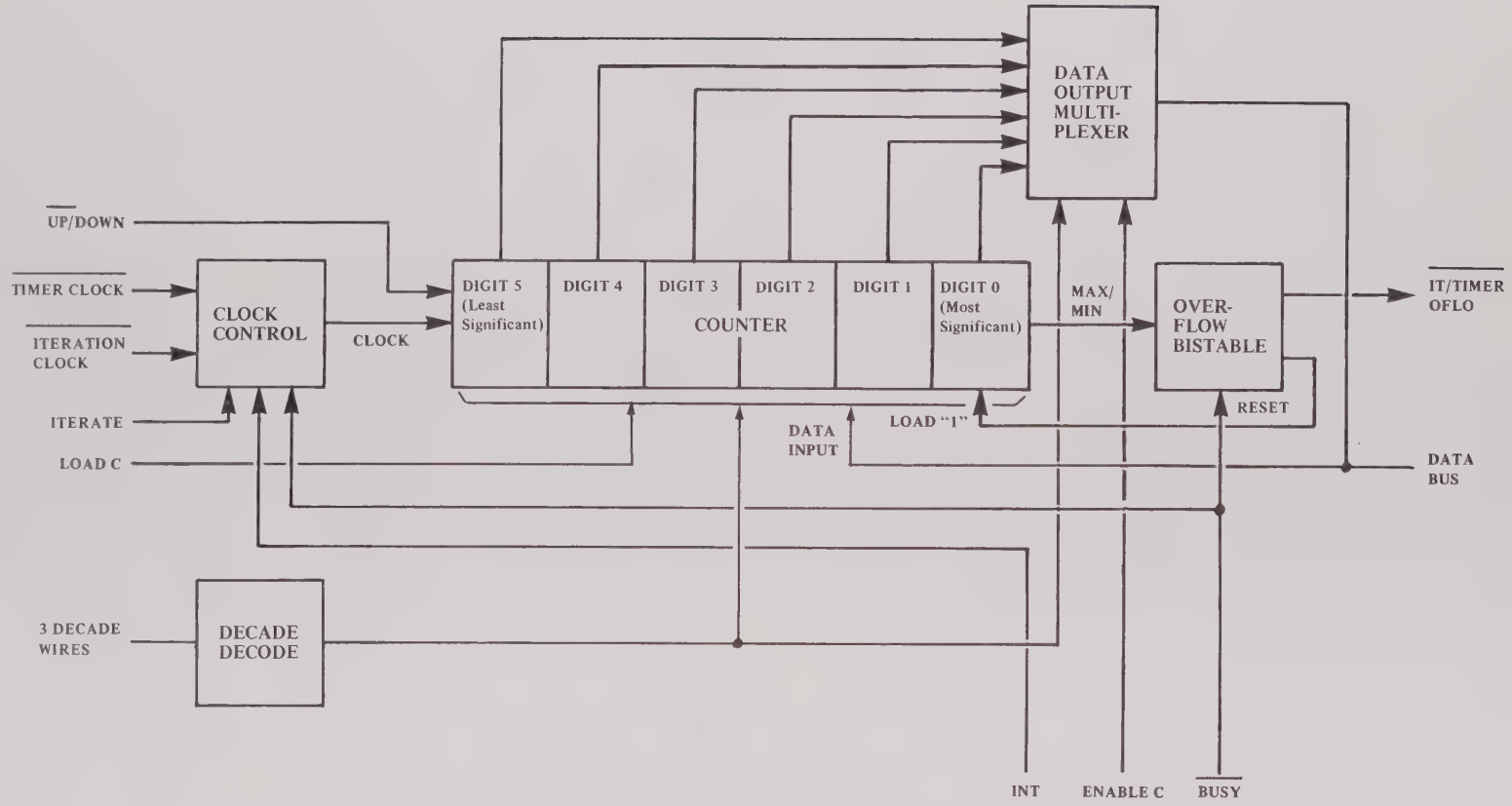
OVERFLOW BISTABLE

This section produces an output $\overline{\text{(TIMER/ITERATION OVERFLOW)}}$ to the sequence logic whenever the part of the counter which is selected counts to zero, either by overflowing (when counting UP) or by counting DOWN to zero. This is used, during iterative operations, to terminate the operation, or, during integration, to initiate an INT.DECSH operation (see "CONTROL OF INTEGRATION"). The signal is derived from the MAX/MIN output from the most significant digit of the counter.

The signal is derived from the MAX/MIN output from the most significant digit of the counter. This is used directly when the counter is counting DOWN (the state zero is the MIN state, i.e. the state immediately before overflow) but is delayed by one clock pulse by a bistable (IC28) when counting UP, as the state zero is reached one pulse *after* the MAX state (i.e. it is the state immediately *after* overflow). The bistable is reset by the $\overline{\text{BUSY}}$ signal at the beginning of every operation.

This section consists of IC28, IC27b, IC20d and e, IC25d and IC23c. Logic is provided so that, during integration (when the INT wire is high), an overflow causes a "one" to be loaded into the most significant digit of the counter. Whenever INT is high, the number "one" is placed on the data inputs of IC12 (this is accomplished by IC18c and IC21b, c and d). When an overflow occurs, a pulse appears on the LOAD input of IC12 (pin 11), causing "one" to be loaded, (accomplished by IC19b). During integration, the counter goes through the states:-

999998
999999
100000
100001
100002
etc.



BOARD 8 BLOCK DIAGRAM
(for more detail refer to circuit diagram)

EXPONENT COUNTER

The exponent counter is situated on board 7. It consists of two 4-bit up/down counters (IC10 and 11), which are used to keep track of the exponents of the contents of registers A and B during shift operations etc. They are known as "Exp A" and "Exp B" respectively. Each of them may be read onto or loaded from the data bus. Two explicit arithmetic unit operations are provided to decrease the contents of either Exp A or Exp B by one ("AExp dec" and "BExp dec"). The operations ATen and BTen also cause the contents of Exp A and Exp B respectively to be decreased by one, in addition to shifting the contents of registers A and B. The operation DTen causes the contents of both Exp A and Exp B to be increased by one, in addition to shifting the contents of registers A and B. If an attempt is made to increment an exponent counter from state 15, it will overflow, and the subsequent state will be zero. The carry out of the counter is lost. Similarly, when counting down, the counters will underflow from zero to 15, and the borrow out of the counter will be lost.

The magnitude of Exp A-Exp B is calculated by a 4-bit adder (IC9) and a set of inverters (IC13) and can be read onto the data bus as Exp C. It cannot of course be loaded explicitly. The sign of Exp C, and a signal which detects that Exp C = 0 (i.e. Exp A = Exp B), can be sensed, via the condition multiplexer, by the control logic. When Exp C is negative (i.e. Exp A > Exp B) it is expressed in 2's complement form.

DETAIL

Loading

If STROBE A and LOAD are high, and the decade number is 7, a pulse on the $\overline{\text{ITERATION CLOCK}}$ wire (which occurs once for every cycle performed by the arithmetic unit) will cause a pulse to appear on the "load" input of IC11 (pin 11) and the digit present on the data bus will replace the current content of Exp A. The old contents are lost (loading of exponent counters is *destructive*). Since an ALoad operation with decade 7 selected will have no effect on register A, Exp A may be loaded exactly as if it were a digit of register A, which is allocated decade number 7.

Loading of Exp B is an exactly analogous process.

Reading

The exponent counters are read onto the data bus via two Quad 2 to 1 line multiplexers (IC8 and IC15). One of Exp A (IC11), Exp B (IC10) or Exp C (IC9) is selected according to the state of the Enable wires (only one of which may be high at a time). It is only read onto the data bus if the decade number is 7. The exponent counters can thus be read exactly as if they were digits in the registers which are allocated decade number 7. It is not necessary to perform a "read cycle, but the control logic does so for the sake of uniformity, and to initiate a data transfer to the store via the store-arithmetic unit data interface.

Counting

The DECSH CMD wire is used as the up/down control wire for both counters. The $\overline{\text{ITERATION CLOCK}}$ signal is used as the clock - the counters are thus incremented or decremented by one for each cycle performed in which they are enabled. Exp A is enabled (by IC20c) if either the ATEN or DECSH CMD wires are high, and Exp B is enabled (by IC20d) if either the BTEN or DECSH CMD wires are high.

Condition Outputs

The sign of Exp C is simply the "carry" output of the adder which computes Exp C. This is the signal EXP C POS. Zero is detected by IC16 a and b and IC17d - this is the signal $\overline{\text{EXP C ZERO}}$.

DECODE LOGIC

The various parts of the arithmetic unit have a total of 22 control wires, the state of which determines the operation which is performed when the arithmetic unit is commanded to "go". Each of these wires is static throughout an operation - they must be set up before the arithmetic unit receives the $\overline{GO}$ pulse, and must remain set up until the operation is completed (i.e the arithmetic unit removes the $\overline{BUSY}$ signal).

The arithmetic unit can perform 32 different types of operation, each of which is allocated to a particular state of the 5 "instruction code" wires, by which the control logic controls the arithmetic unit, and each of which requires that the 22 control wires are set up to a particular state. The 32 different states of the 5 instructions codes wires are translated into the corresponding 32 states of the 22 control wires by the Decode Logic.

This is situated on board 7, and comprises two 256 bit read only memories, (IC1 and 2), each of which receives the 5 instruction code wires as its address and produces 8 of the 22 control wires. The remaining 6 of the control wires are produced by a one-in-ten decoder (IC3, type 7442) and a number of gates.

The truth table for the Decode Logic, together with the instruction names and the names of the 22 control wires is shown in Table A.

TABLE A DECODE OUTPUTS

INSTRUCTION CODE	IC1								IC2								IC3								INSTRUCTION NAME
	1/1000	CLEAR	LOAD	STOP CODE B	STOP CODE A	STROBE B	STROBE A	INH SGN CH	MPX 1 CMD	MPX 2	MPX 4A	MPX 4B	ADD B CMD	ADD A CMD	UP/DOWN	ITERATE	INT	DELAY/INT	LOAD C	DECSH	ATEN	BTEN			
																CONTROL SIGNAL									
0	0	1	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0			BAdd
1	0	1	0	1	1	0	1	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0			BSub
2	0	1	0	1	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0			AAdd
3	0	1	0	1	1	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0			ASub
4	1	1	0	1	1	0	1	0	1	0	1	1	1	0	0	1	0	0	0	0	0	0			Log
5	1	1	0	0	1	1	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0			Exp
6	1	1	0	1	0	1	1	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0			Polar
7	1	1	0	0	1	1	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0			Cartes
8	0	0	0	1	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0			AClear
9	0	0	0	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0			BClear
10	0	1	1	1	1	0	1	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0			ALoad
11	0	1	1	1	1	1	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0			BLoad
12	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0			Read
13	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0			AExp dec
14	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1			BExp dec
15	0	1	1	1	1	0	1	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0			AOne load
16	0	1	0	1	1	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0			AX-9
17	0	0	0	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0			AInv
18	0	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0			Comp
19	0	1	0	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0			ADouble
20	0	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0			BDouble
21	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0			Swap
22	0	1	0	1	0	1	0	0	0	1	1	1	0	1	0	1	0	0	0	0	0	0			XDivide
23	0	1	0	1	0	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0			YDivide
24	0	1	0	1	1	1	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0			Int
25	0	0	0	1	1	0	0	0	1	1	1	1	1	1	0	0	1	1	0	0	0	0			MDelay
26	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	1	0	0	0			DTen
27	0	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0			CLoad
28	0	0	0	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0			CTen
29	0	0	0	1	1	1	1	0	1	1	1	0	1	1	0	0	0	0	0	0	1	0			ATen
30	0	0	0	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	1			BTen
31	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0			BOne Load

Condition Multiplexer

The control logic can sense the state of a total of 32 different wires in the instrument, by means of conditional instructions. The names and meanings of these wires are shown in INTRODUCTION TO THE CONTROL LOGIC, Table B. The sixteen wires in Group 2, which include all those originating within the arithmetic unit, appear on board 7, and are multiplexed to two wires by means of two 8-to-1 line multiplexers. The 8 wires with numbers between 0 and 7 are multiplexed onto the ARITH COND 1 wire by IC5. The 8 wires with numbers between 8 and 15 are multiplexed onto the ARITH COND 2 wire by IC6. Both of these multiplexers are addressed by the least significant three instruction code wires.

Arith Bistables

Two bistables are provided for use by the control logic as memory elements or as a counter. The bistables are arranged as a two-bit "down" counter, and are controlled by the 6th instruction code wire (the "32" bit of the instruction code). The counter is clocked by the BUSY signal only if this wire is high - it is thus clocked one for each arithmetic unit instruction with a code between 32 and 63 (these 32 codes are otherwise exact duplicates of the codes between 0 and 31).

The state of the least significant bistable (which changes state for every operation with a code between 32 and 63) can be sensed as condition 11, and the most significant bistable (which changes state when the least significant bistable changes from 0 to 1) can be sensed as condition 12. No means of resetting the bistable explicitly is provided.

Input System Settling Delay

A monostable (IC7) is provided for use as a delay after changing the input range (during the autorange sequence) or the input system mode (during a reject bias measurement) to ensure that the input system has recovered from any overload state before commencing a measurement. The monostable is triggered by a pulse output from the control logic (CMD DELAY) and its output can be sensed as a condition 6. Its period is nominally 30mSec.

THE ARITHMETIC REGISTERS

Introduction

Most of the arithmetic performed by the arithmetic unit is accomplished by two registers, Register A and Register B. Each consists of an identical board, numbered 5, occupying positions 5 and 6 respectively in the instrument. They are referred to in this account as "the board" or "the register" (not to be confused with the term "shift register", which refers to a single integrated circuit), and where signal names are given they refer to Register A, with the corresponding name for Register B in brackets, if different.

Each board can store indefinitely a 9 digit BCD number, with sign, and can add or subtract another 9 digit number ("input data") from it. The board works on a "digit by digit" basis. The input data is added to the register contents one digit at a time, starting with the least significant digit. Each digit requires one clock pulse, to perform a complete addition or subtraction thus requires 9 clock pulses. Clock pulses always occur in groups of nine at a rate of 5MHz. Each group corresponds to an arithmetic unit "Cycle". Iterative operations are made up of many additions or subtractions, and thus require many cycles.

Data Timing

The least significant digit of the input data is accepted by the board on the first clock pulse of the cycle, and the most significant digit on the last clock pulse. All sources of input data must be timed accordingly. The least significant digit must be present before and until the first clock pulse (when it is accepted by any board that is using it as input data). It is then replaced by the second digit in readiness for the second clock pulse, and so on, until the ninth (last) clock pulse, when the most significant digit is accepted by the board, and is replaced by the least significant digit in preparation for the next cycle.

Control Wires

The board is controlled by a number of control wires. These can be divided into two groups:

a) Sequential control wires.
These originate on board 4 ("Sequence logic"), and may change pulse by pulse through the cycle. They include the clock signal mentioned above.

b) Static control wires.
Most of these originate on board 7 ("Decode logic"). They do not change during a cycle (or only at points in the cycle where they are not active).

These are detailed in Table 1.

a) Sequential control wires.
1. $\overline{\text{PRECLOCK}}$
2. $\overline{\text{CPO}}$
3. OUTPUT LATCH STROBE
4. MPX STROBE
5. MPX ADDR 1

b) Static control wires.

	REGISTER A	REGISTER B (if different)
1.	SGN V	
2.	SGN (SIN)	SGN (COS)
3.	ADD A CMD	ADD B CMD
4.	ADD B CMD	ADD A CMD
5.	POS B	POS A

6.	$\overline{\text{INH. SGN CH.}}$	
7.	$\overline{\text{LOAD}}$	
8.	$\overline{\text{DECSH}}$	
9.	$\overline{\text{DEC 6}}$	
10.	$\overline{\text{CLEAR}}$	
11.	$\overline{\text{DEC 6}}$. $\overline{\text{DEC 7}}$	
12.	MPX ADDR 2	
13.	MPX ADDR 4A	MPX ADDR 4B
14.	STROBE A	STROBE B
15.	INT.	

TABLE 1

Data Communication

Data is communicated to and from the iteration counter or the store, one digit at a time, via the arithmetic unit data bus. This is a two directional, negative logic, four wire, data bus. Each register is provided with an "enable" wire. When the enable wire for a register is high, a previously selected digit is read from the register onto the bus, where it will remain until it has been accepted by the receiving device (this may take up to 512μ Sec. for the store). When the enable wire is low, a zero is read onto the bus (i.e. four logic highs, as the bus operates in negative logic), freeing the bus for use by other registers. The digit which is read onto the bus is selected by means of the three "Decade" wires.

Internal Organisation

With the single exception of the data output latch, the board is composed entirely of synchronous logic. All bistables and shift registers are driven by the same clock signal, which is derived by a single inverter from the $\overline{\text{PRECLOCK}}$ signal. The heart of the board is a loop consisting of four 8 bit shift registers, a set of four bistables, and a BCD processor section (See Fig. 1.). The processor is divided into two parts, each consisting of combinational logic only, which are separated by the set of bistables. The four shift registers operate in parallel, so that data is shifted out of them into the processor section four bits (one BCD digit) at a time. Each digit passes through the shift registers, through the first part of the processor and into the set of bistables, then through the second part of processor and back into the shift registers. There are nine stages in this loop, so that at the end of a group of nine clock pulses, each digit has returned to its "home" position, having passed through all nine stages, and through the processor.

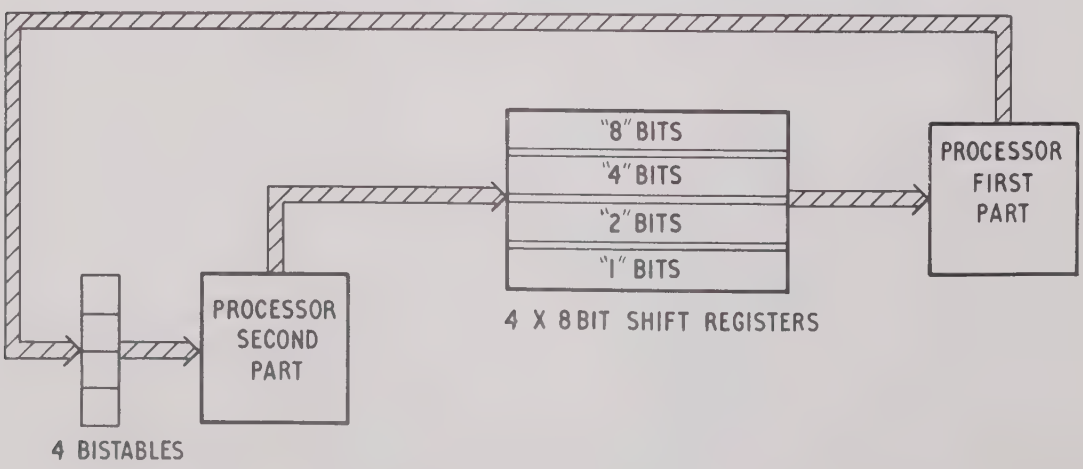


Fig. 1 Arithmetic Register Central Loop.

Processor (See Fig.2)

The first part of the processor performs a binary addition or subtraction of a digit of the data from the corresponding digit of the register contents, and computes the resulting decimal carry or borrow bit. Subtractions are performed by forming the ones complement of the input data (performed by a set of exclusive - OR gates) before it is added to the register contents. The intermediate result formed by the first part of the processor enters the set of bistables where it is stored until the next clock pulse. An "abnormal carry" bistable (ABN CARRY) stores the carry information and an ADD' bistable stores the add/subtract mode until the next clock pulse. A "carry/borrow" bit is computed from the outputs of these two bistables for addition to the next digit processed. No carry or borrow into the least significant digit is allowed - the "carry/borrow" bit is forced to the state marked "normal" when this digit is being processed (see table 2).

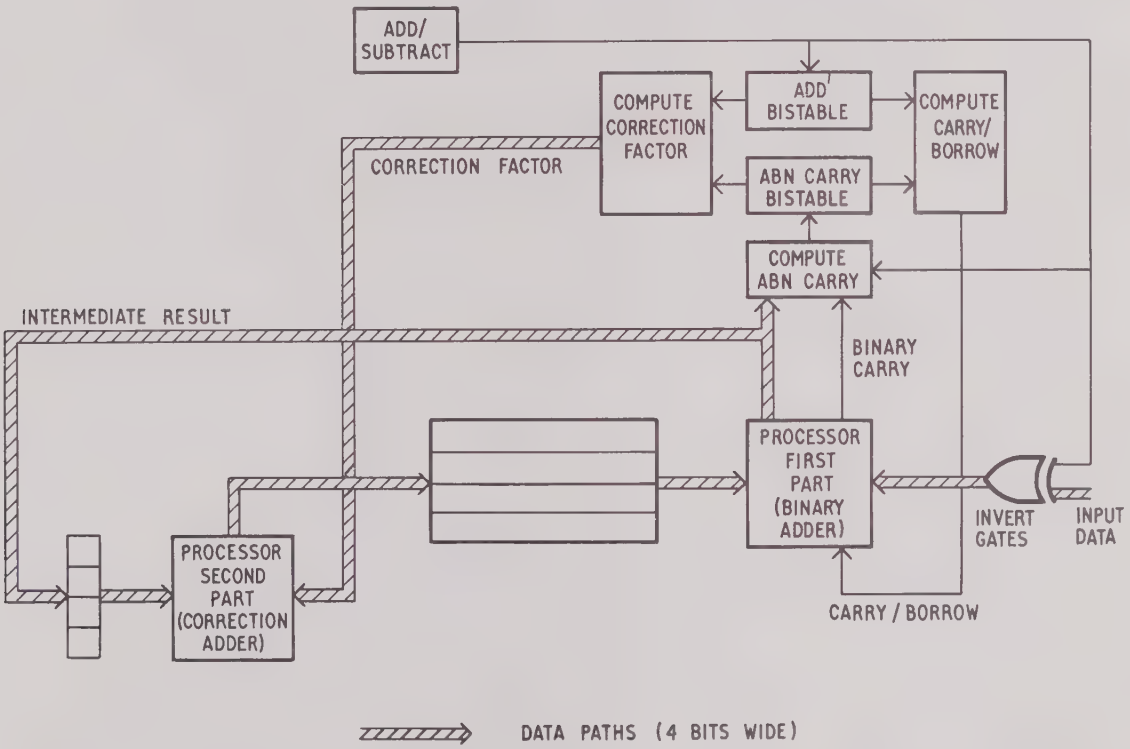


Fig. 2 Processor.

			CARRY/BORROW	MEANING	ABN CARRY	CORRECTION FACTOR
ADD	sum <	10	0	normal	0	0
	sum ≥	10	1	carry one	1	6
SUBRACT	difference <	0	0	borrow one	1	10
	difference ≥	0	1	normal	0	0

TABLE 2

The second part of the processor is a "correction adder". It adds a correction factor computed from the output of the ABN CARRY and ADD bistables to the intermediate result, to give the final result. The "16" bit of this result is ignored, and it is then a true BCD digit (see table 3).

	ADD						SUBTRACT						
COLUMN	1	2	3	4	5		6	7	8	9	10	11	
	0	0	0	0	0		- 10	6	0	10	16	0)	
	1	0	0	1	1		- 9	7	0	10	17	1)	
	2	0	0	2	2		- 8	8	0	10	18	2)	
	3	0	0	3	3		- 7	9	0	10	19	3)	
	4	0	0	4	4		- 6	10	0	10	20	4)	
	5	0	0	5	5		- 5	11	0	10	21	5)	borrow
	6	0	0	6	6		- 4	12	0	10	22	6)	
	7	0	0	7	7		- 3	13	0	10	23	7)	
	8	0	0	8	8		- 2	14	0	10	24	8)	
	9	0	0	9	9		- 1	15	0	10	25	9)	
	10	1	6	16	0)		0	16	1	0	16	0	
	11	1	6	17	1)		1	17	1	0	17	1	
	12	1	6	18	2)		2	18	1	0	18	2	
	13	1	6	19	3)		3	19	1	0	19	3	
	14	1	6	20	4)		4	20	1	0	20	4	
	15	1	6	21	5)	carry	5	21	1	0	21	5	
	16	1	6	22	6)		6	22	1	0	22	6	
	17	1	6	23	7)		7	23	1	0	23	7	
	18	1	6	24	8)		8	24	1	0	24	8	
	19	1	6	25	9)		9	25	1	0	25	9	

TABLE 3

COLUMN

1	Input data and carry bit added to register contents. Equal to intermediate result (output of processor first part).
2	New CARRY/$\overline{\text{BORROW}}$ bit ("1" = carry).
3	Correction factor.
4	Sum of intermediate result and correction factor
5	Final result (ignoring "16" bit).
6	Input data and borrow bit subtracted from register contents.
7	Intermediate result (output of processor first part).
8	New CARRY/$\overline{\text{BORROW}}$ bit ("0" = borrow).
9	Correction factor.
10	Sum of intermediate result and correction factor.
11	Final result (ignoring "16" bit).

Data Outputs

Three outputs are provided from each board for use as input data. Since digits are processed one at a time, each having ten times the significance of the previous digit, the significance of a data output can be determined by choosing the timing of the digit relative to the clock. Normally the least significant digit is produced in time to be accepted as input data on the first clock pulse of a cycle and so on. In this case the data output has a significance of "1". If the output is taken from a point one

stage later in the shift register, the data will be delayed by one clock pulse (i.e. the least significant digit is produced in time to be accepted on the second clock pulse of a cycle, etc.) and will have a significance of "10". If the digits are advanced by taking from a point earlier on the shift register, the significance of the data is reduced by ten times for each clock pulse advance. The three data outputs provided have significances of "10", "1" and "1/1000".

Input Multiplexer

Each board can select one of 8 sources from which to take its input data. This is performed by a set of four 8-to-1 line multiplexers. The multiplexers have a 3 bit address. The '1' and '2' bits are common to the two boards - separate "4" bits are provided, to allow a certain amount of flexibility in the selection of data sources. The "2" and "4" bits of the multiplexer address are static control wires - the "1" bit is a sequential control wire, although it is only used as such during the "integrate" operation, when its function is to switch the input data source from the "1" digit of the SIN and COS signals to the "10" digit, after the first clock pulse of the cycle. For the allocation of multiplexer addresses, see table 4.

Mpx Address	Register A	Register B
0	SIN 1	COS 1
1	SIN $\overline{10}$	COS $\overline{10}$
2	10A	10B
3	DATA BUS	DATA BUS
4	LOG. CONST.	B/1000
5	B/1000	A/1000
6	A	B
7	B	A

TABLE 4

Note: The multiplexer address shown here refers to the signals appearing on boards 5 and 6. It should be noted that the "1" bit of the MPX ADDRESS is inverted with respect to the MPX 1 CMD wire originating on board 7.

Strobe Gates

A set of gates is provided to enable none, some, or all of the nine digits of the input data to be added. The "pattern" of digits added to the register is determined by the MPX STROBE wire, a sequential control wire common to both boards. Separate static control wires (STROBE A and STROBE B) are provided, allowing neither, either or both registers to accept input data. When the input data is disabled, zero is added to or subtracted from the register contents, and the multiplexer address is of course irrelevant.

Clear Gates

A set of gates is provided which allows the register contents to be discarded before entering the processor section of the board. These are controlled by the $\overline{\text{CLEAR}}$ wire, a static control wire common to both boards. If this wire is low, the input data is added to or subtracted from zero. This enables the register contents to be cleared or inverted.

Decsh Gates

A set of four AND-OR-INVERT gates is provided so that the data in the register can be made to bypass the processor and the set of four bistables. This means that each digit requires only 8 clock pulses to reach its "home" position. Thus at the end of the cycle each digit has reached one position further, its weight being reduced by a factor of ten. This has the overall effect of shifting the contents of the register down one digit position, dividing its magnitude by ten. The AND-OR-INVERT gates are controlled by the $\overline{\text{DECSH}}$ wire, a static control wire common to both boards. Logic is provided to ensure that the most significant (9th) digit is equal to zero after a Decsh operation (during an integration operation - i.e. while the INT wire is high - the most significant digit will be made equal to 9 after a Decsh operation, if the register contents are negative, as they will be in 10's complement form).

Add Gates

Normally the add/subtract mode of the board is controlled directly by the ADD A CMD (ADD B CMD) wire. However, if both ADD A CMD and ADD B CMD are low, the add/subtract mode is controlled by the sign of the register contents, such that the board will only subtract if the contents are negative. This feature is provided for use by the Complement operation (the only operation for which both ADD A CMD and ADD B CMD are low).

During Integration (i.e. while the INT wire is high) the add/subtract mode is controlled by the SGN SIN (SGN COS) and SGN V wires. An exclusive - OR gate forms the product of these two signals, which then determines the add/subtract mode for the cycle to be performed.

Sign Bistable

Each board is provided with a sign bistable to keep track of the sign of the register contents during add and subtract (and integrate) operations. In order for the bistable to operate correctly, it is necessary for the register contents to be in 10's complement form if negative. The bistable works on the principle that an examination of the sign of the register contents, and whether they are being added or subtracted, will determine whether an operation will change the contents in a direction towards zero or away from it. If the contents will change in a direction away from zero, or if the board is not adding or subtracting, a sign change is impossible, and any change of state of the bistable is inhibited. If the contents of the register will change in a direction towards zero, the new sign can be determined from the ABN CARRY signal (see table 5). Due to propagation delay considerations, the new sign must be computed by a complex set of gates from the data outputs of the first part of the processor, rather than from the ABN CARRY signal. A static control wire which will inhibit changes of the sign bistables regardless of other conditions, is provided ($\overline{\text{INH. SGN. CH.}}$).

SIGN OF REGISTER CONTENTS	SIGN OF INPUT DATA	ADD/SUBTRACT MODE	SIGN CAN CHANGE	ABN CARRY	NEW SIGN
+	+	ADD	NO	(0	-
+	+	SUBTRACT	YES	(1	+
+	-	SUBTRACT	NO	(0	-
+	-	ADD	YES	(1	+
-	-	ADD	NO	(0	-
-	-	SUBTRACT	YES	(1	+
-	+	SUBTRACT	NO	(0	-
-	+	ADD	YES	(1	+

TABLE 5

It is assumed that input data in an addition or subtraction operation is coming from the other register. The signal POS B (POS A) indicates whether it is positive or negative. During integration (i.e. when the INT wire is high), this signal is disabled, as the value of SIN (COS) is always regarded as positive (negative values are obtained by subtracting the positive value).

The sign bistables may be loaded from the "1" bit of the data bus if the LOAD, DEC 6 and STROBE A (STROBE B) wires are high, and the $\overline{\text{INH. SGN. CH.}}$ wire is low.

Output Latch

A four bit latch is provided to enable any one of digits 0 to 5 to be latched during a cycle for subsequent reading onto the data bus. It is supplied with a strobe pulse (OUTPUT LATCH STROBE), whose position in the cycle is determined by the DECADE wires, from board 4. The contents of the latch are read onto the data bus if the ENABLE A (ENABLE B) and $\overline{\text{DEC 6}}$ $\overline{\text{DEC 7}}$ wires are high. The contents of the sign bistable are read onto the "1" bit of the data bus if the ENABLE A (ENABLE B) and DEC 6 wires are high - they are also available as a separate signal, POS A (POS B), for use by the control logic (via the condition multiplexer).

Dec 9 Zero Gate

An output signal $\overline{\text{DEC 9 A ZERO}}$ ($\overline{\text{DEC 9 B ZERO}}$) is provided to indicate to the control logic (via the condition multiplexer) whether the 9th digit of the register contents is zero.

Delay Bistables

All signals present on the edge - connector of the board are timed so that events associated with the least significant digit occur on the first clock pulse of the cycle, and so on. Static control signals, which affect all 9 digits, change between cycles. However, they may affect various different points on the central loop of the register. The least significant digit may not reach the point affected (the "control point") until one or two clock pulses after the beginning of the cycle, and the most significant digit may not reach it until one or two clock pulses after the beginning of the succeeding cycle, which may not occur for some time after the cycle in question. Bistables are necessary to delay the arrival of control signals until the least significant digit of the register contents arrives at the control point, and to store the signals until the most significant digit has passed this point on the loop.

Bistables in this category are:

1)	Set of 4 input data bistables	(one clock pulse delay)
2)	ADD bistable	(one clock pulse delay)
3)	ADD' bistable	(two clock pulses delay)
4)	INH. SGN. CH bistable	(one clock pulse delay)
5)	CLEAR bistable	(one clock pulse delay)
6)	DECSH bistable	(two clock pulses delay)

Some control signals, while they are static in the sense that their effect is constant for all 9 digits, are not maintained for the whole of the cycle. Bistables which store these signals must not be allowed to change state until the end of the cycle, if the input signal should change. This is achieved by routing the outputs of these bistables back to their inputs for all clock pulses when they are not permitted to change state. The bistables to which this applies are:

1) ADD bistable
2) DECSH bistable
3) POS A (POS B) bistable (slightly different, in that it is the ABN CARRY information that is not maintained, rather than the control signals)

The signal $\overline{\text{CPO}}$ is provided to indicate the first clock pulse of the cycle. A signal indicating the second pulse is generated on the board (CPO'). These signals are used to control changes of state of the bistables shown above, and also to control sections of the board which require a mode change

at some point in the cycle, e.g.:

1) Carry and borrow must be inhibited for the first digit.
2) Decsh gates must force the 9th digit to zero or nine.

Logic Convention

All data inputs and outputs to the board are in negative logic. However, some parts of the board (principally the processor and the set of 4 bistables) operate in positive logic. These are indicated in fig. 3.

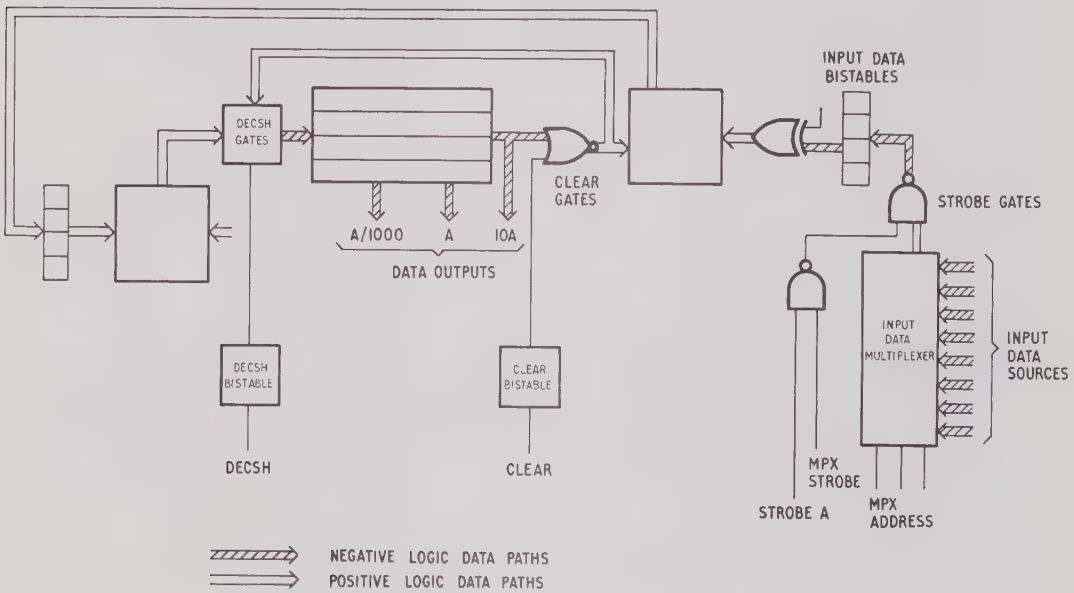


Fig. 3 Logic Data Paths.

INTRODUCTION TO SEQUENCE LOGIC

The "sequence logic" is situated on board 4. Its function is to interlock the arithmetic unit and control logic timing, and to produce all clocks and sequential signals required by the arithmetic unit. The operation of the sequence logic will be described for all operations except for integration, in this chapter.

The sequence logic can be subdivided into the following sections.

1. Clock generator
2. Sequential control signal generator
3. Clock enable logic
4. Sequence control

1. Clock Generator

The clock input to the board is a continuous 10MHz clock. A continuous 5MHz clock is derived from this by a bistable operating as a divide by 2 stage. The 5MHz clock drives most of the bistables in the sequence logic.

The $\overline{\text{PRECLOCK}}$ signal is also generated by this section of the board. This signal is used as a clock by the arithmetic register boards (5 and 6). It is a train of pulses, occurring in groups of 9, at a rate of 5MHz. The pulses within a single arithmetic unit operation are continuous, but the number of pulses is always a multiple of 9. Incomplete cycles are not allowed. An 8 bit shift register is used to ensure that pulses occur in groups of 9. The shift register is clocked by the $\overline{\text{PRECLOCK}}$ signal. Its input (named $\overline{\text{CPO}}$) is high if any one of its stages is set to "0". If all the 8 stages are set to "1", the input ($\overline{\text{CPO}}$), which will become the state of the first stage after the next clock pulse, is low. There are thus 9 states through which the shift register can pass:-

STAGE	1	2	3	4	5	6	7	8	Input ($\overline{\text{CPO}}$)
	1	1	1	1	1	1	1	1	0
	0	1	1	1	1	1	1	1	1
	1	0	1	1	1	1	1	1	1
	1	1	0	1	1	1	1	1	1
	1	1	1	0	1	1	1	1	1
	1	1	1	1	0	1	1	1	1
	1	1	1	1	1	0	1	1	1
	1	1	1	1	1	1	0	1	1
	1	1	1	1	1	1	1	0	1

The $\overline{\text{PRECLOCK}}$ signal is generated by a bistable clocked by the 10MHz clock. The output of this bistable follows the 5MHz clock if either the $\overline{\text{CPO}}$ signal or the CLOCK ENABLE signal is high. If both these signals are low, the output of the PRECLOCK bistables is permanently high (i.e. the clock stops). This means that the clock can only stop with the shift register in the first state shown above, which occurs once every 9 pulses. The number of clock pulses which occur in a group must be a multiple of 9. The CLOCK ENABLE signal is used to initiate or maintain a group of clock pulses. If the signal is removed the clock will stop when the next multiple of 9 is reached. A signal (C in P) indicating that a cycle is in progress, is produced for use by the "sequence control" section.

2. Sequential Control Signal Generator

A number of "sequential control signals" are produced whose state depends upon the stage in the cycle which has been reached. These signals are used by other parts of the arithmetic unit. They are generated from the outputs of the shift register and the position of the "0" in the shift register, if any, indicates which of the 9 clock pulses has been reached.

The signals are (See Fig. 1):

	SIGNAL	USED BY BOARDS
1.	$\overline{\text{CPO}}$	5,6
2.	ITERATION CLOCK	7,8
3.	MPX STROBE	5,6
4.	OUTPUT LATCH STROBE	5,6
5.	MPX ADDR 1	5,6
6.	LOG CONST. $\overline{8}$	5
7.	LOG CONST. $\overline{4}$	5
8.	LOG CONST. $\overline{2}$	5
9.	LOG CONST. $\overline{1}$	5

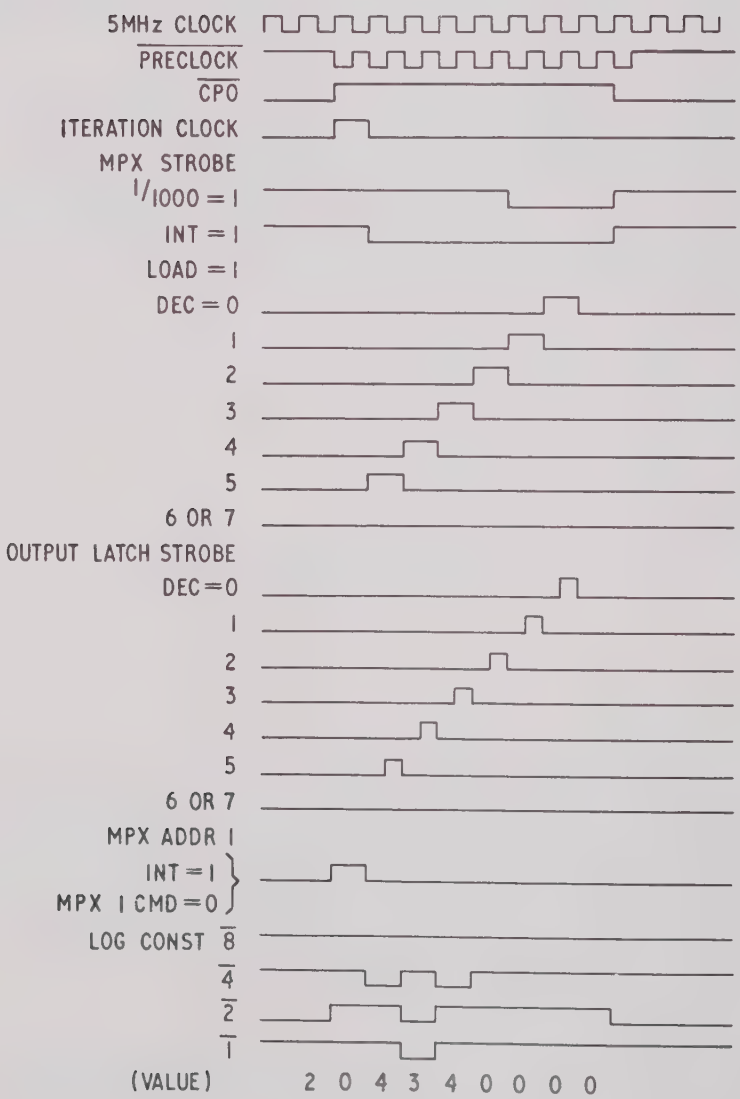


Fig. 1 Arithmetic Unit Timing Diagram.

3. Clock Enable Logic

This section is composed of gates only. Its function is to initiate an arithmetic unit operation, and to terminate it when the appropriate conditions are satisfied. It has a number of modes of operation, which are selected by the STOP CODE A and STOP CODE B wires.

a) Single cycle operations. (See Fig. 2).
STOP CODE A = high
STOP CODE B = high
Nine clock pulses are produced in this mode. The CLOCK ENABLE wire remains high for one clock pulse (200nSec) only to initiate a cycle,. and the operation finishes at the end of the cycle.

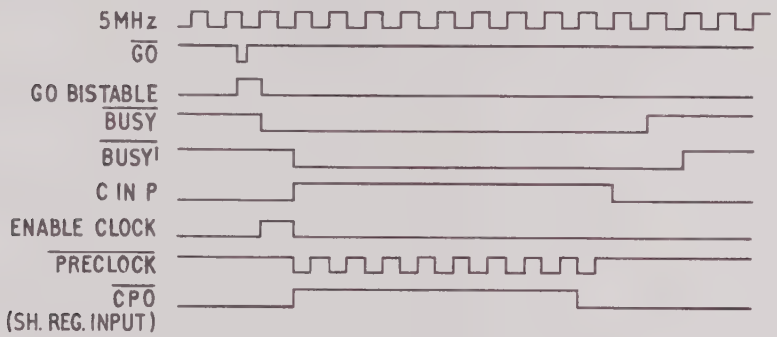


Fig. 2 Single Cycle Operation

b) Iterative operations. (See Fig. 3).
i) STOP CODE A = high
STOP CODE B = low

In this mode cycles continue until either the TIMER/ITERATION OFLO wire goes low or the ABN CARRY A wire goes high. When either of these things happens, the CLOCK ENABLE wire goes low, and the clock stops at the end of the cycle. Since the clock can only finish at one point in the cycle, the state of the ABN CARRY A wire is irrelevant except between the last clock pulse of one cycle and the first clock pulse of the next (the level of this signal may in fact change at any or all clock pulses). Change of state of the TIMER/ITERATION OFLO signal should occur slightly after the 2nd clock pulse of the cycle (i.e. slightly after the iteration clock edge).

If the TIMER/ITERATION OFLO signal is low when an operation is requested, no cycles will be performed. The ABN CARRY signal however is ignored for the first cycle (this signal may have been left high by the previous operation) - if ITERATION/TIMER OFLO is high before the operation, at least one cycle must occur.

ii) STOP CODE A = low
STOP CODE B = high

In this mode the conditions which must be satisfied to terminate the operation are the same as (i) above, except:-
ABN CARRY B is used in place of ABN CARRY A
Both ABN CARRY B and TIMER/ITERATION OFLO are ignored for the first cycle. In this mode, at least one cycle must occur.
In both (i) and (ii) above, the TIMER/ITERATION OFLO signal is assumed to be present if DECADE number 6 or 7 is selected. In this case the operation will stop after no cycles (case (i)) or one cycle (case (ii)) respectively. This is a precaution only, to prevent infinitely long operations when the wrong DECADE is selected.

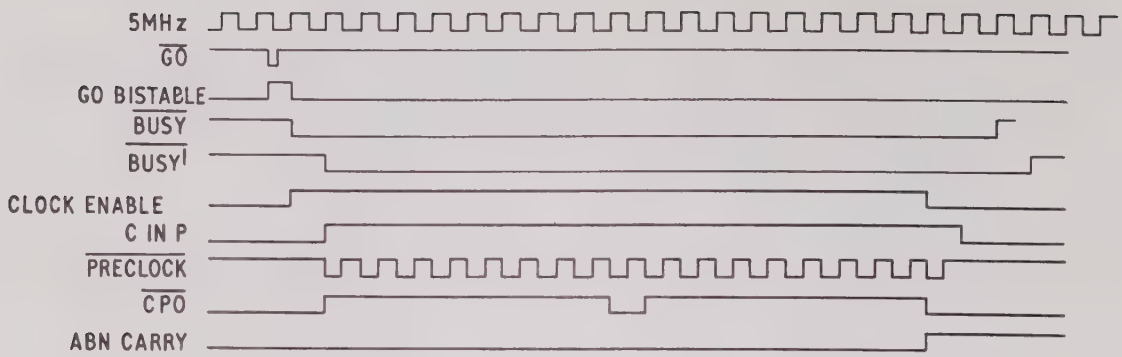


Fig. 3(a) Iterative Operation (Stopped By ABN CARRY).

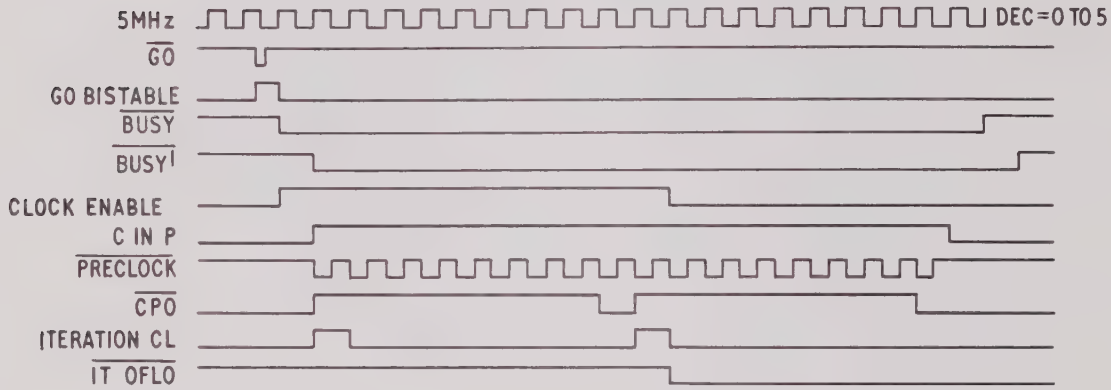


Fig. 3(b) Iterative Operation (Stopped By IT OFLO).

c) STOP CODE A = low
STOP CODE B = low

This mode is never used.

4. Sequence Control

This section consists of a number of bistables and gates. Its function is to accept the command to perform an operation (the GO pulse) from the control logic, generate the BUSY signal which indicates to the control logic that an arithmetic unit operation is in progress, and to instruct the clock enable logic to initiate the operation.

The GO pulse is accepted by an RS bistable and stored until the next 5MHz clock pulse. The BUSY bistable is then set (a maximum of 200nS after the leading edge of the GO pulse), which causes the BUSY signal to the control logic to go low, inhibiting further control logic action. The RS bistable is reset at this point, provided that the GO pulse has finished (otherwise it will remain set until GO pulse finishes). A BUSY' bistable follows the BUSY bistable with 1 clock pulse (200nSec) delay. The BUSY' signal is used to enable most of the conditions for terminating operations (the TIMER/ITERATION OFLO signal is permanently enabled if STOP CODE B = low, causing no cycles to be performed under certain conditions - see 3, b, i above). Initially BUSY = low and BUSY' = low. The termination conditions are thus disabled. When BUSY goes high, the CLOCK ENABLE wire will go high, (except in the special case mentioned in 3, b, i above) and the operation will commence. On the next clock pulse, BUSY' will go high, enabling the termination conditions. The operation will continue until these conditions are met.

The BUSY bistable remains set as long as the C in P bistable is set. When the operation is finished, the C in P bistable will reset, and the following clock pulse, the BUSY bistable will reset, allowing the $\overline{\text{BUSY}}$ wire to the control logic to go high. The control logic will then procede to the next instruction, and the arithmetic unit will remain quiescent until the next $\overline{\text{GO}}$ pulse. The BUSY bistable cannot reset if CLOCK ENABLE is high. This prevents it from resetting at the beginning of an operation, before the C in P bistable is set.

INTRODUCTION TO THE CONTROL LOGIC

The arithmetic unit is only capable of performing simple operations autonomously. Each stage in the calculation of the results or in the calculation of the new frequency in a frequency sweep, involves many such steps. Other parts of the instrument also require commands at various points in the measuring sequence (see Table A). It is the function of the control logic to issue these commands in the correct sequence to perform whatever action is requested by the touch keys. In fact the instrument is performing a continuous sequence of operations whenever it is switched on, as the state of waiting for a command from the front panel involves a sequence of examining in turn each touch key from which a command could come.

Sections requiring commands from control logic.	Nature of commands
1. Arithmetic unit	32 arithmetic operations, including data transfers to and from the store.
2. Store	Read and write commands in conjunction with the arithmetic unit (see above)
3. Keyboard display	Update local display data buffer from the appropriate store location.
4. Keyboard	a. Disable keyboard while the machine is running b. Switch SINGLE button to OFF at the end of the measurement. c. Switch sweep button to OFF at the end of a frequency sweep, or if the synchroniser (1185) is in use.
5. Autorange counter	a. The counter used to control the input range in the autorange sequence is set to the 10mV range at the beginning of the sequence. b. Increment autorange counter.
6. Input system	Various modes may be selected: a. Measure bias b. Reject bias
7. Peripherals	The machine indicates to any peripherals that may be attached (plotter, teletype, computer etc.) that the results are ready to be accepted.

Table A Control Logic Functions

The control logic follows a program of 1024 instructions. Each of these is an 8 bit word, - they are stored in four 2048 bit read-only memory IC's (Board 11, IC's 19, 24, 32, 39). The program includes jump instructions, sub-routines and conditional instructions. An instruction may be internal to the control logic (e.g. a jump instruction, or an instruction setting an internal memory bistable), or may involve one or more other sections of the machine. Conditional instructions are used so that changes in the state of other sections of the instrument may affect the path taken by the control logic through the program. The control logic can monitor the state of various counters and bistables within itself in the same way (see Table B).

ARITHMETIC UNIT CONDITIONS

Group	No.	Name	Source	Meaning
2	0	$\overline{\text{DEC 9 ZERO A}}$	Register A (Board 5)	Is the 9th decade of register A equal to zero?
2	1	$\overline{\text{DEC 9 ZERO B}}$	Register B (Board 6)	Is the 9th decade of register B equal to zero?
2	2	EXP C POS	Exponent counter (Board 7)	Is EXP C positive? (i.e. EXP B $\geqslant$ EXP A)
2	3	$\overline{\text{EXP C ZERO}}$	Exponent counter (Board 7)	Is EXP C equal to zero? (i.e. EXP B = EXP A)
2	4	POS A	Register A (Board 5)	Are the contents of register A positive?
2	5	POS B	Register B (Board 6)	Are the contents of register B positive?
2	11	ARITH BS 1	Board 7	Is bistable no.1 set?
2	12	ARITH BS 2	Board 7	Is bistable no.2 set?

TOUCH KEY CONDITIONS

Group	No.	Name	Source	Meaning
1	4	Measure mode X	Touch keys	Which of keys X, Y, Y/X
1	5	Measure mode Y	Touch keys	is selected?
1	11	Measure sequence SINGLE	Touch keys	Which of keys STOP, SINGLE, RECYCLE
1	12	Measure sequence RECYCLE	Touch keys	is selected?
1	10	Sweep ON	Touch keys	Which of keys OFF, HOLD,
1	9	Sweep DOWN/ HOLD	Touch keys	UP, DOWN is selected?
1	13	Sweep LOG	Touch keys	Which of keys LIN LOG is selected?
1	15	ENTER FREQUENCY	Touch keys	Has the ENTER key been pressed? (with FREQUENCY selected)
1	14	ENTER VOLTS	Touch keys	Has the ENTER key been pressed? (with OUTPUT VOLTS selected)
1	3	REJECT BIAS	Touch keys	Is the REJECT BIAS key selected?

TABLE B

INTERNAL CONDITIONS

Group	No.	Name	Source	Meaning
2	7	INPUT X/$\overline{Y}$	Input channel bistable	Are the input channel relays set to X or Y?
2	13	$\overline{\text{MEASURE BIAS}}$	Measure bias bistable	Is "measure bias" mode selected?
1	2	MARKER BISTABLE	Marker bistable	Is the bistable set? (local memory element)
1	8	SWEEP BISTABLE	Sweep bistable	Is the bistable set? (i.e. is this the first measurement of a frequency sweep)?
1	6	ARITH DEC 8	Arithmetic decade counter	Is the 8 bit of the counter set?

MISCELLANEOUS EXTERNAL CONDITIONS

Group	No.	Name	Source	Meaning
1	0	INPUT RELAY FLAG	Input relays	Are the relays in the process of changing?
1	1	AUTORANGE OVERLOAD	Autorange logic (Board 17)	Has integration been terminated by an overload during an autorange measurement?
2	10	OVERLOAD	Autorange logic (Board 17)	Has overload occurred during this measurement?
2	14	PERIPHERAL FLAG	Peripherals	Have all peripherals which may be attached to the instrument finished receiving the results, or programming the instrument?
2	9	SYNCHRONISER FLAG	Synchroniser (1185) option	Is the measurement value of the period of the synchronising signal ready for processing?
2	8	$\overline{\text{LEAD/LAG}}$	Lead/lag link (Board 7)	Is the instrument set to measure lead angles (link present) or lag angles (link absent)?
2	6	Input system settling delay	Delay Monostable (Board 7)	Is the delay monostable set? This allows a 30mS period for the input system to settle after altering the range during an autorange sequence.
1	7	STORE OVERLOAD	Store	Is the overload bit set in the currently addressed store word?
2	15	SPARE FLAG		

In order to control the states of other sections of the instrument, various pulse and level outputs are available (see Table D).

PULSE OUTPUT	DESTINATION	FUNCTION
GO	Arithmetic unit	Initiate instruction specified by INSTRUCTION CODE lines.
RESET RANGE	Autorange counter	Reset range to 10mV at beginning of autorange sequence.
$\overline{\text{INC. RANGE}}$	Autorange counter	Increment range during autorange sequence.
$\overline{\text{CHANGE FREQ}}$	a) Keyboard display b) Peripherals	Update local display data buffer from frequency or volts location in store. Indicates that results are ready to be output.
$\overline{\text{MOS STORE WRITE}}$	Store	Write current data bus digit into store.
$\overline{\text{RESET OVERLOAD}}$	Autorange logic	Reset overload bistable at beginning of measurement.
$\overline{\text{CMD DELAY}}$	Delay monostable (Board 7)	Initiate input system settling delay (used after changing range in autorange sequence).
$\overline{\text{RESET SWEEP}}$	Touch keys.	Reset sweep buttons to OFF.

LEVEL OUTPUT	DESTINATION	FUNCTION
INSTRUCTION CODE	Arithmetic unit	5 lines - select one of 32 arithmetic unit operations. 1 line - enable programmable arithmetic unit bistables.
DECADE NO.	Arithmetic unit	Select one of 8 decades.
$\overline{\text{MEASURE BIAS}}$	Arithmetic unit Input system	Select "measure bias" mode.
X/$\overline{\text{Y}}$ RELAYS	Input channel relays	Select channel X or Y
$\overline{\text{COMPUTE}}$	a) RUN lamp b) Peripherals	RUN lamp is on when $\overline{\text{COMPUTE}}$ = 0 Control data sourcing and data receiving peripherals.
$\overline{\text{RUN}}$	Touch keys	Disable keyboard while $\overline{\text{RUN}}$ = 0 Switch SINGLE button off at end of measurement.
ENABLE $\overline{\text{A}}$, $\overline{\text{B}}$, C.	Arithmetic unit	Enable arithmetic unit register A, B or C to write data onto the arithmetic unit data bus.

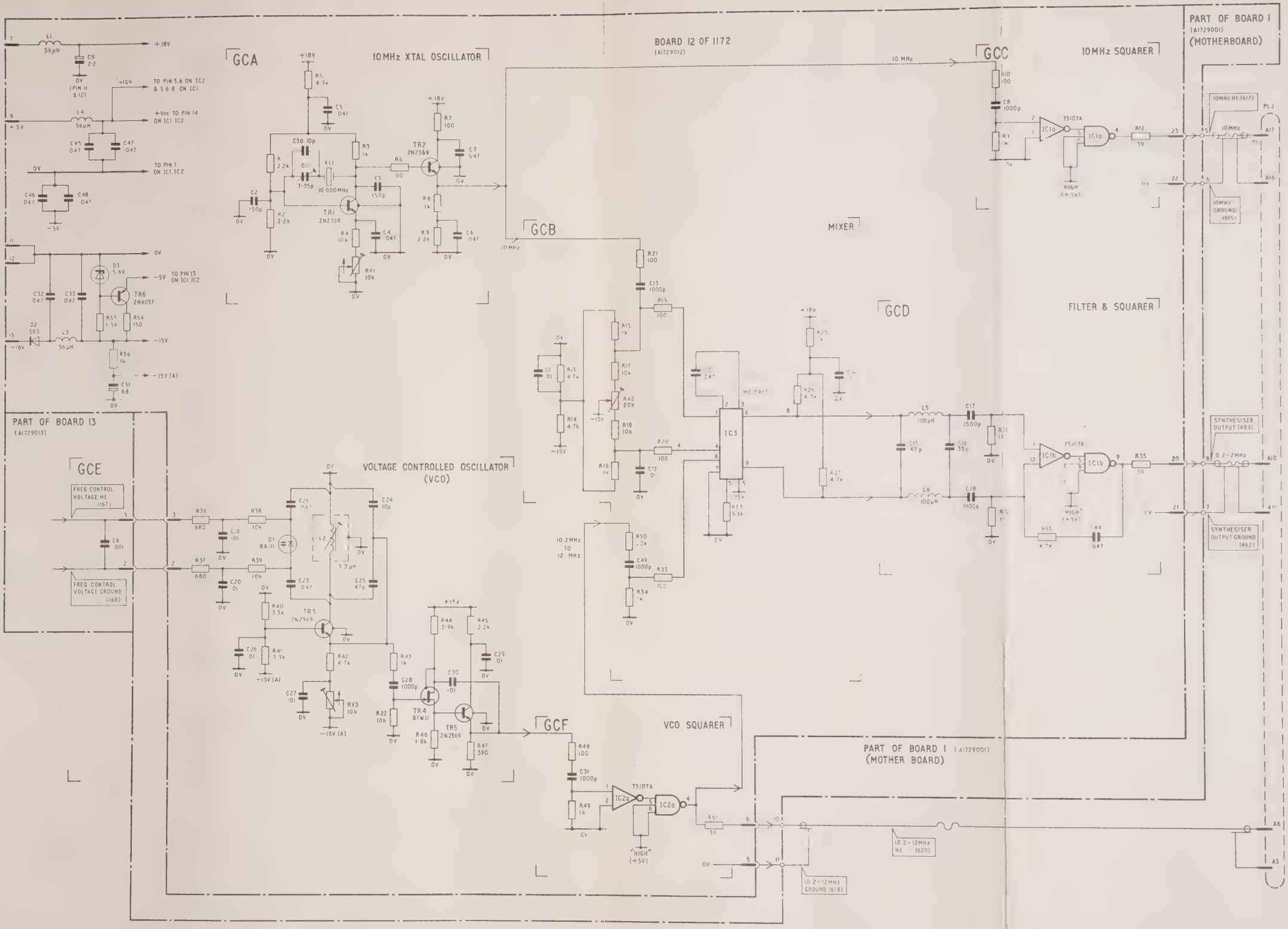
Table D Control Logic Output Signals

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 1

SOURCE	SIG No.	DESTINATION
5	168	
5	167	
	617	2
	615	2
	489	50
	462	
	620	3
	619	3



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2.

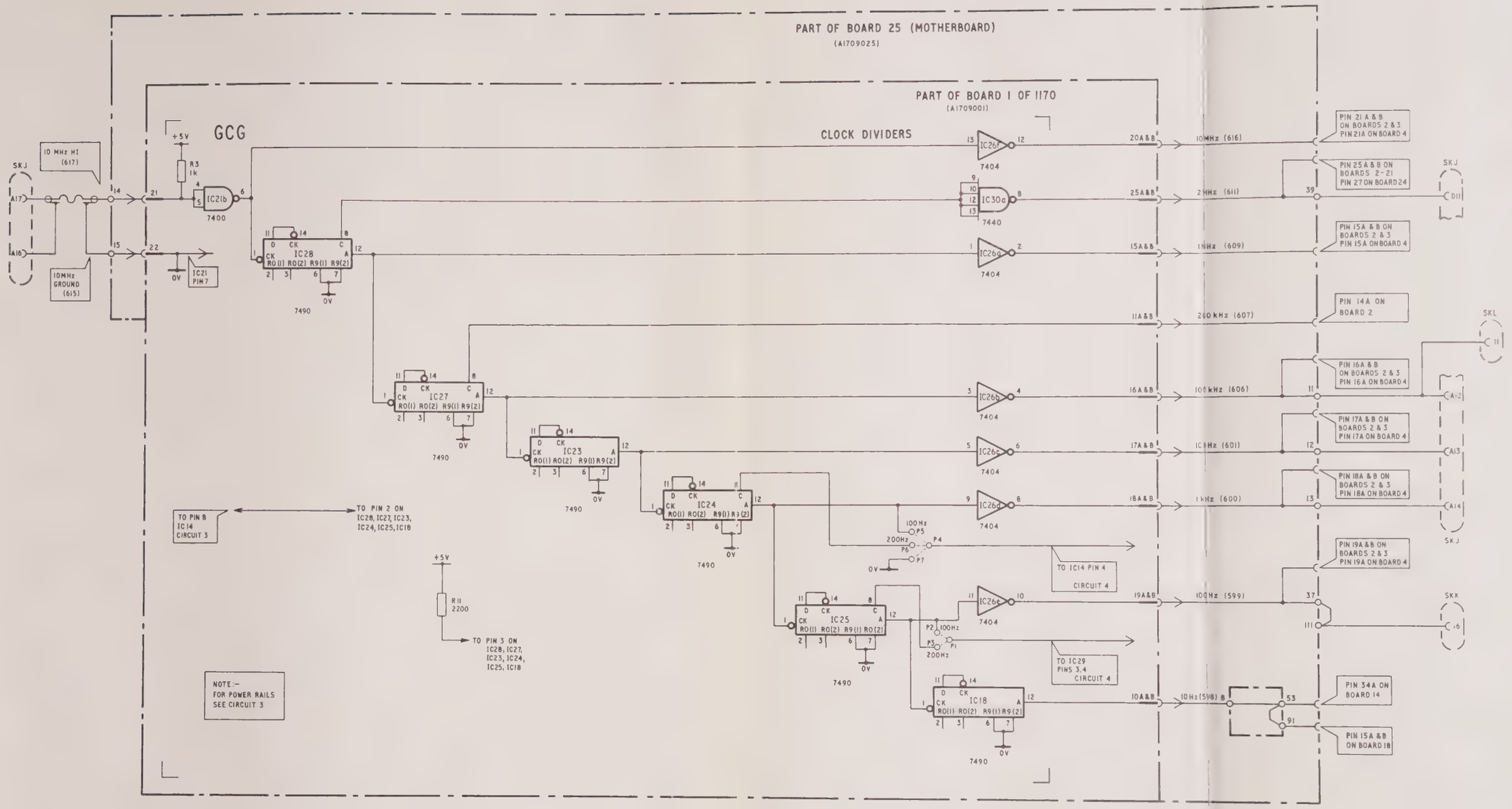
Use this diagram for instruments with 1172 Serial No. 200541 onwards; for instruments with earlier serial numbers refer to diagram 2A.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 2

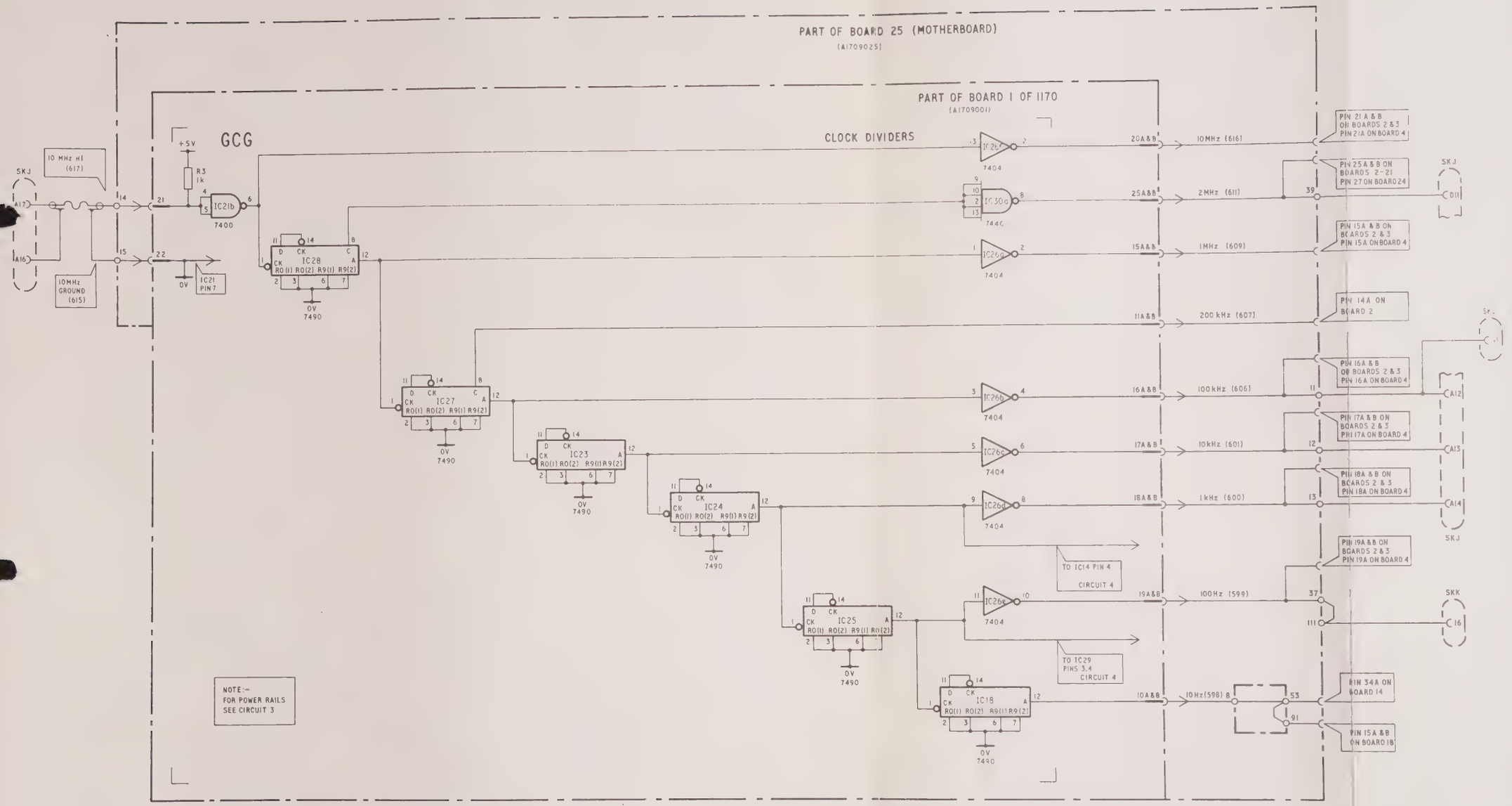
SOURCE	SIG No.	DESTINATION
1	615	
1	617	
	616	
	611	21.25.50.54.58.65.66.69.70.72.
	609	
	607	
	606	
	601	
	600	
	599	
	598	



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 2A

Use this diagram for instruments with numbers earlier than 1172 Serial No. 200541.



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 3 See page 1.3.10

The MOS store data output lines (339 to 342) define the frequency required from the synthesiser output in circuit 1. These data are loaded into the counters (IC10 etc.) which are then counted down by the 10.2 to 12MHz output from circuit 1. If the synthesiser output is correct the outputs to circuit 4 will be 100Hz; or higher or lower if not.

Outputs 359, 360 and 26 are related to the generator circuit (14) and not to the synthesiser circuits as are the other components.

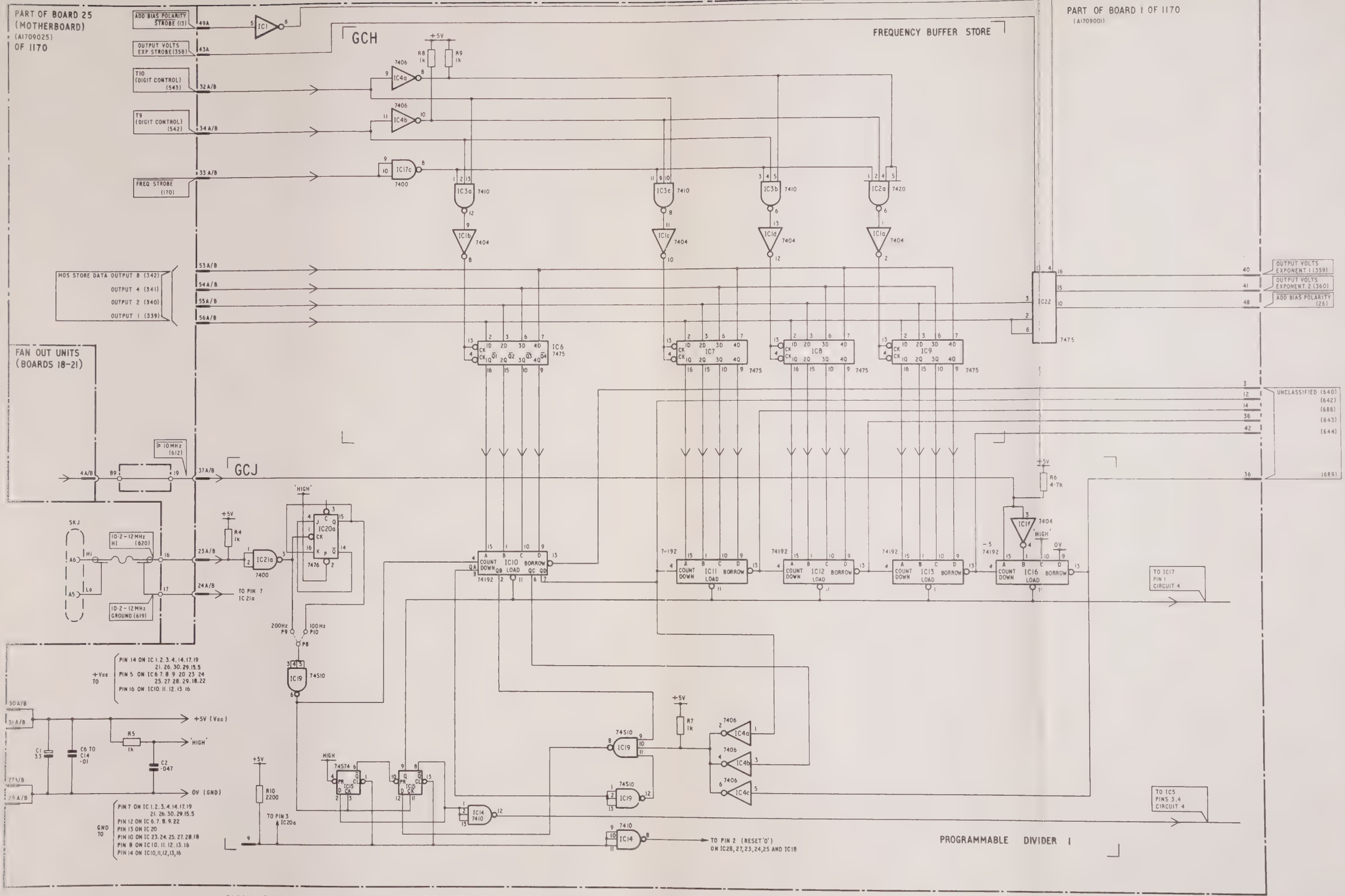
Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 3

SOURCE	SIG No.	DESTINATION
1	619	
1	620	
	612	
66	339	50.63.69.70.71.72.74.
66	340	50.63.70.71.72.74.
66	341	50.63.70.71.72.73.74.
66	342	50.63.70.71.72.74.
69	1[illegible]0	
67	542	[illegible]9
67	543	[illegible]9
69	358	
69	1[illegible]3	
	359	[illegible]4
	360	[illegible]4
	26	[illegible]5
	640	
	642	
	688	
	643	
	644	
	689	

Use this diagram for instruments with 1172 Serial No. 200541 onwards; for instruments with earlier serial numbers refer to diagram 3A.



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 3A

Use this diagram for instruments with numbers earlier than 1172 Serial No. 200541.

PART OF BOARD 25
(MOTHERBOARD)
(AI709025)
OF 1170

PART OF BOARD 1 OF 1170
(AI709001)

FREQUENCY BUFFER STORE

GCH

ADD BIAS POLARITY STROBE (13) — 49A
OUTPUT VOLTS EXP STROBE (358) — 43A
T10 (DIGIT CONTROL) (543) — 32A/B
T9 (DIGIT CONTROL) (542) — 34A/B
FREQ. STROBE (170) — 33A/B

MOS STORE DATA OUTPUT 8 (342)
OUTPUT 4 (341)
OUTPUT 2 (340)
OUTPUT 1 (339)
53A/B
54A/B
55A/B
56A/B

OUTPUT VOLTS EXPONENT 1 (359) — 40
OUTPUT VOLTS EXPONENT 2 (360) — 41
ADD BIAS POLARITY (26) — 48

UNCLASSIFIED (640) (642) (688) (643) (644) (689)

FAN OUT UNITS
(BOARDS 18-21)

≥ 10MHz (612)
4A/B — 37A/B

SKJ
10-2-12MHz HI (620)
10-2-12MHz GROUND (619)
23A/B
24A/B
TO PIN 7 IC21a

+Vcc TO
PIN 14 ON IC 1.2.3.4.14.17.19 21.26.30
PIN 5 ON IC 6.7.8.9.20.23.24 25.27.28.29
PIN 16 ON IC10.11.12.13.16
PIN 4 ON IC15

30A/B
31A/B
+5V (Vcc)
'HIGH'
C1 0·1
C6 TO C14 ·01
R5 1k
C2 0·1
27A/B
28A/B
0V (GND)

GND TO
PIN 7 ON IC 1.2.3.4.14.17.19 21.26.30
PIN 12 ON IC 6.7.8.9.
PIN 13 ON IC 20
PIN 10 ON IC 23.24.25.27.28.29
PIN 8 ON IC 10.11.12.13.16
PIN 11 ON IC15

TO IC17 PIN 1 CIRCUIT 4

TO IC5 PINS 3,4 CIRCUIT 4

PROGRAMMABLE DIVIDER

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 4 See page 1.3.10

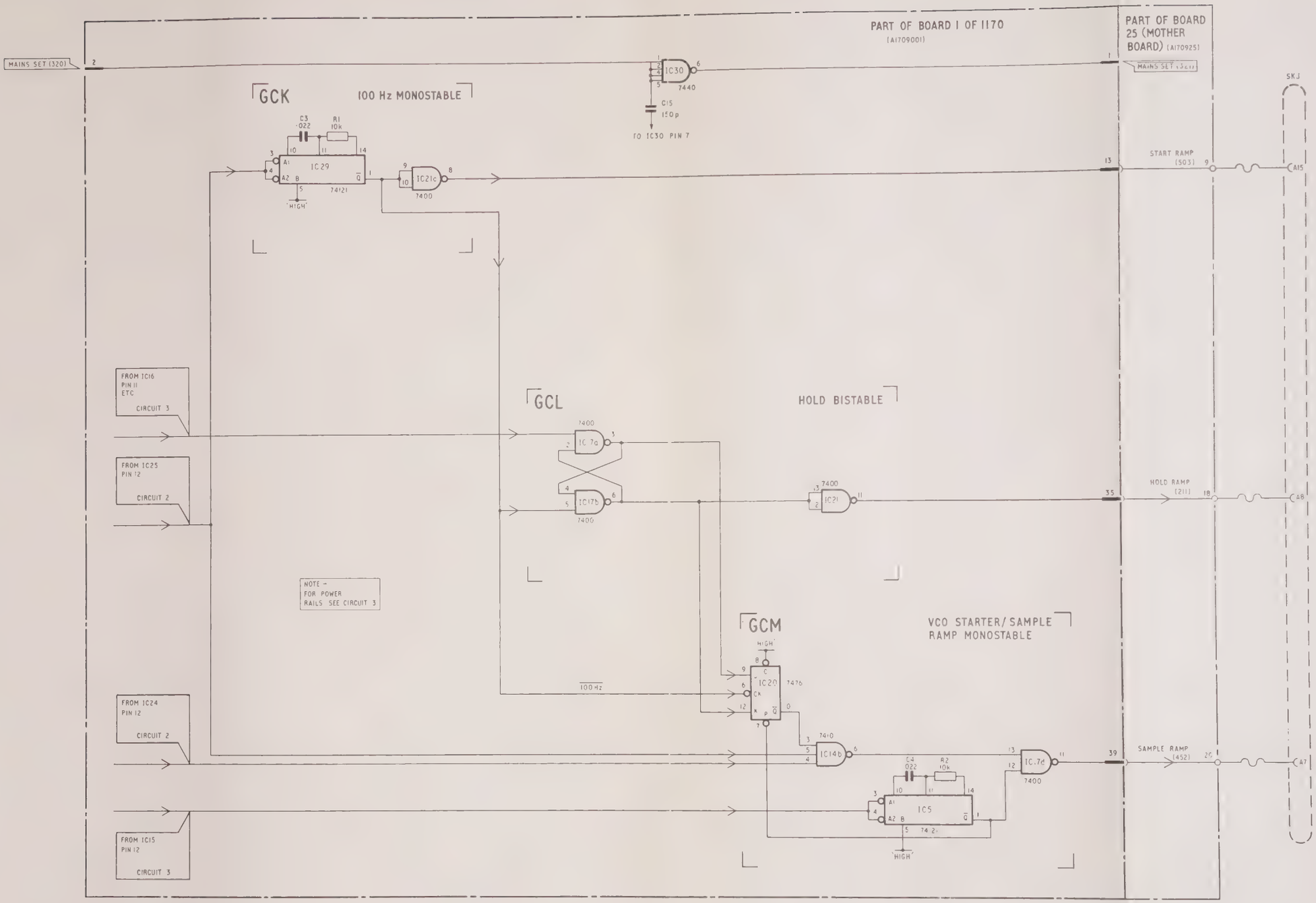
This circuit provides the three shaped outputs used in circuit 5. See block diagram for the timing of these outputs.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 4

SOURCE	SIG No.	DESTINATION
44	320	
	321	30.34.50.58.66.
	503	5
	211	5
	452	5



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 5

SOURCE	SIG No.	DESTINATION
4	452	
4	211	
4	503	
	167	
	168	

1.4 Circuit Diagrams

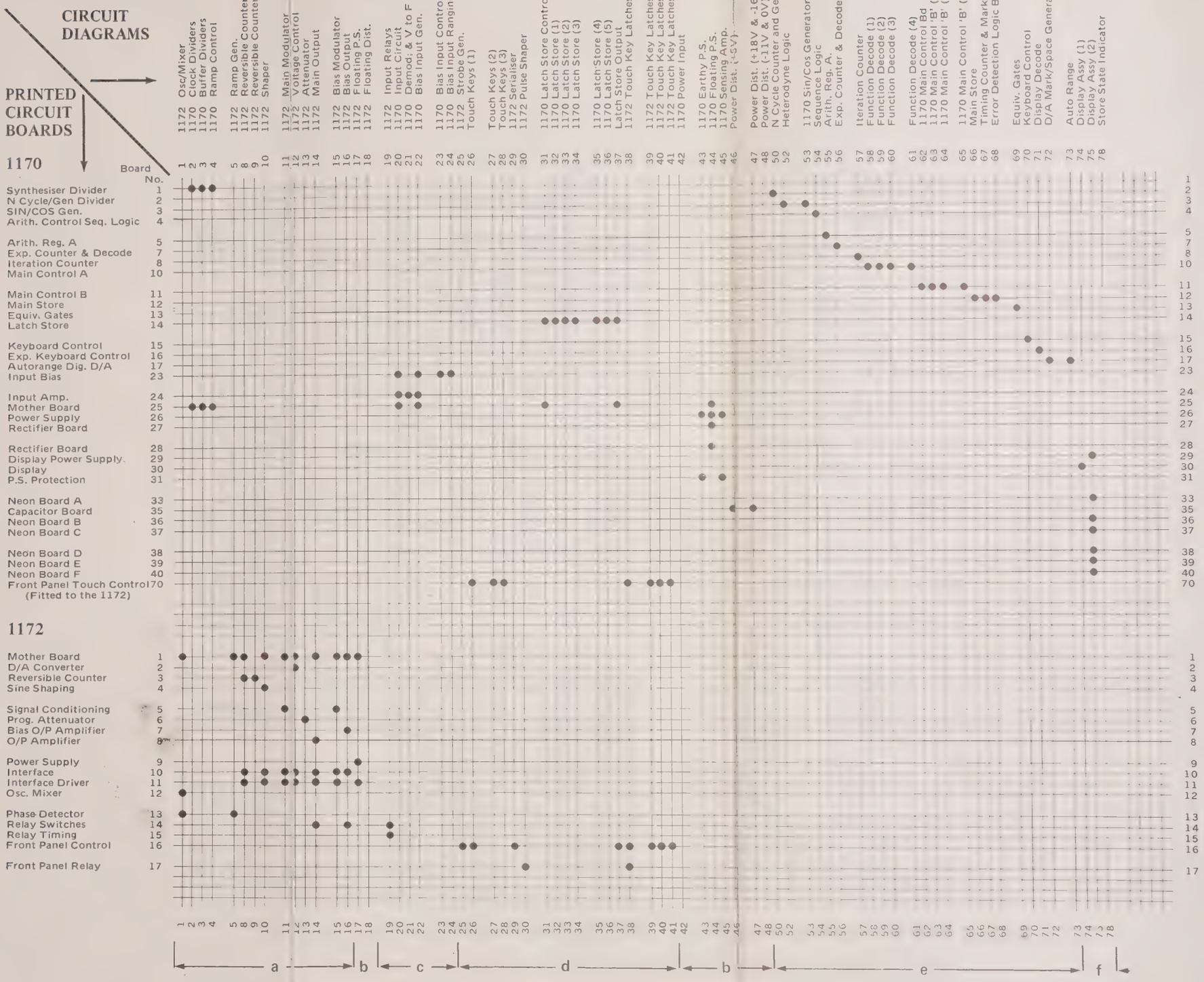
Most of the circuit diagrams have been laid out with groups of components which perform certain functions confined within imaginary blocks. The corners of the blocks are included in the drawing. The purpose of the blocks is to assist the reader to follow the functional paths throughout the system.

Some diagrams, notably those in the digital section, are not functionally divided. This is due to the nature of the signals within these boards making the functional tracing of signal paths a practical impossibility. Fault finding on these boards (pcb 2 - 5, 7, 8, 10 - 13 and 15 - 17) should not be attempted.

Immediately following this introduction is a chart showing the relation between these circuit diagrams and the printed circuit boards. The purpose of this chart is to provide the link between the funtional circuit diagrams and the physical location of the components. It also indicates the major functional areas of the instrument.

List of Circuit Diagrams

1	1172 Osc/Mixer
2	1170 Clock Dividers
3	1170 Buffer Dividers
4	1170 Ramp Control
5	1172 Ramp Gen.
8	1172 Reversible Counter Cont.
9	1172 Reversible Counter
10	1172 Shaper
11	1172 Main Modulator
12	1172 Voltage Control
13	1172 Attenuator
14	1172 Main Output
15	1172 Bias Modulator
16	1172 Bias Output
17	1172 Floating P.S.
18	1172 Floating Dist.
19	1172 Input Relays
20	1170 Input Circuit
21	1170 Demod; & V to F
22	1170 Bias Input Gen.
23	1170 Bias Input Control
24	1170 Bias Input Ranging
25	1172 Strobe Gen.
26	Touch Keys (1)
27	Touch Keys (2)
28	Touch Keys (3)
29	1172 Serialiser
30	1172 Pulse Shaper
31	1170 Latch Store Control
32	1170 Latch Store (1)
33	1170 Latch Store (2)
34	1170 Latch Store (3)
35	1170 Latch Store (4)
36	1170 Latch Store (5)
37	Latch Store Output
38	1172 Touch Key Latches (1)
39	1172 Touch Key Latches (2)
40	1172 Touch Key Latches (3)
41	1172 Touch Key Latches (4)
42	1170 Power Input
43	1170 Earthy P.S.
44	1170 Floating P.S.
45	1170 Sensing Amp.
46	Power Dist. (+5V)
47	Power Dist. (+18V & −16V)
48	Power Dist. (−11V & 0V)
50	N Cycle Counter and Generator Divider.
52	Heterodyne Logic
53	1170 Sin/Cos Generator
54	Sequence Logic
55	Arith. Reg. A.
56	Exp. Counter & Decode
57	Iteration Counter
58	Function Decode (1)
59	Function Decode (2)
60	Function Decode (3)
61	Function Decode (4)
62	1170 Main Control Bd.
63	1170 Main Control 'B' (1)
64	1170 Main Control 'B' (2)
65	1170 Main Control 'B' (3)
66	Main Store
67	Timing Counter & Marker Bit Generator
68	Error Detection Logic Board 12.
69	Equiv. Gates.
70	Keyboard Control
71	Display Decode
72	D/A Mark/Space Generator
73	Auto Range.
74	Display Assy (1)
75	Display Assy (2)
76	LED Display (1)
77	LED Display (2)
78	Store State Indicator



This chart shows the relation between the printed circuit boards and the circuit diagrams of the 1170 series.

The board numbers are repeated on the right-hand side of the chart for convenience and likewise the circuit numbers at the bottom of the chart.

The main purpose of the chart is to allow easy cross-reference between the circuit diagrams in Section 1 of the Servicing Manual and the pcb information in Section 2.

The spots indicate which numbers of circuit diagrams should be consulted for each pcb. For instance, the chart shows that the circuit diagram of board 10 of the 1170 will be found on circuits No. 58 to 61.

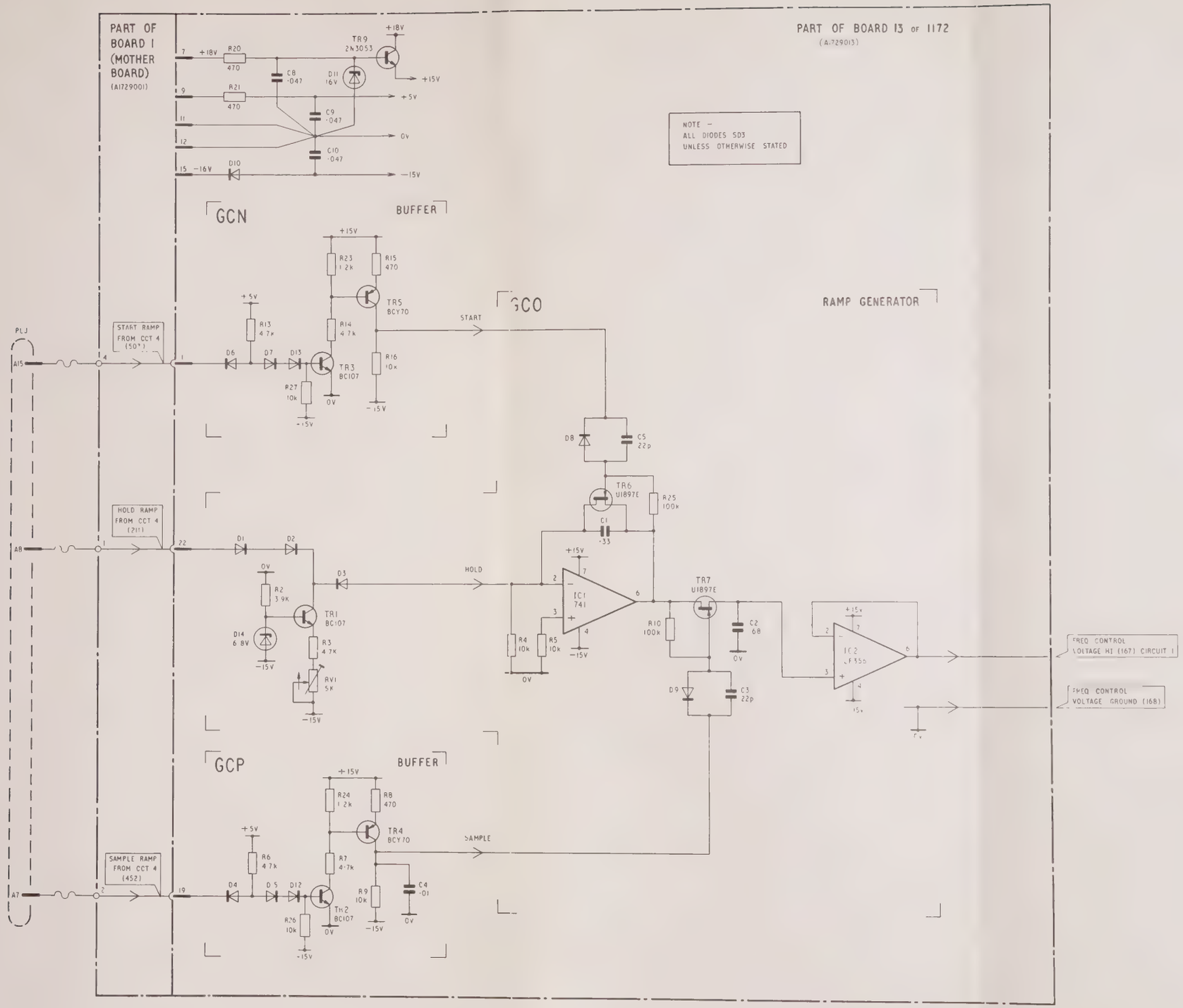
It should be noted that as far as the circuits are concerned the 1172 and 1177 are identical, except that certain parts of the 1172 are not included on the 1177.

The major functional areas of the instrument are shown by the following key.

- **a** GENERATOR
- **b** POWER SUPPLIES
- **c** INPUT SYSTEM
- **d** SELECT LATCHING
- **e** DIGITAL SECTION
- **f** DISPLAY

LED DISPLAY pcb's 49 and 50 are shown on circuit diagrams 76 and 77

1170 CIRCUIT DIAGRAM ALLOCATION CHART



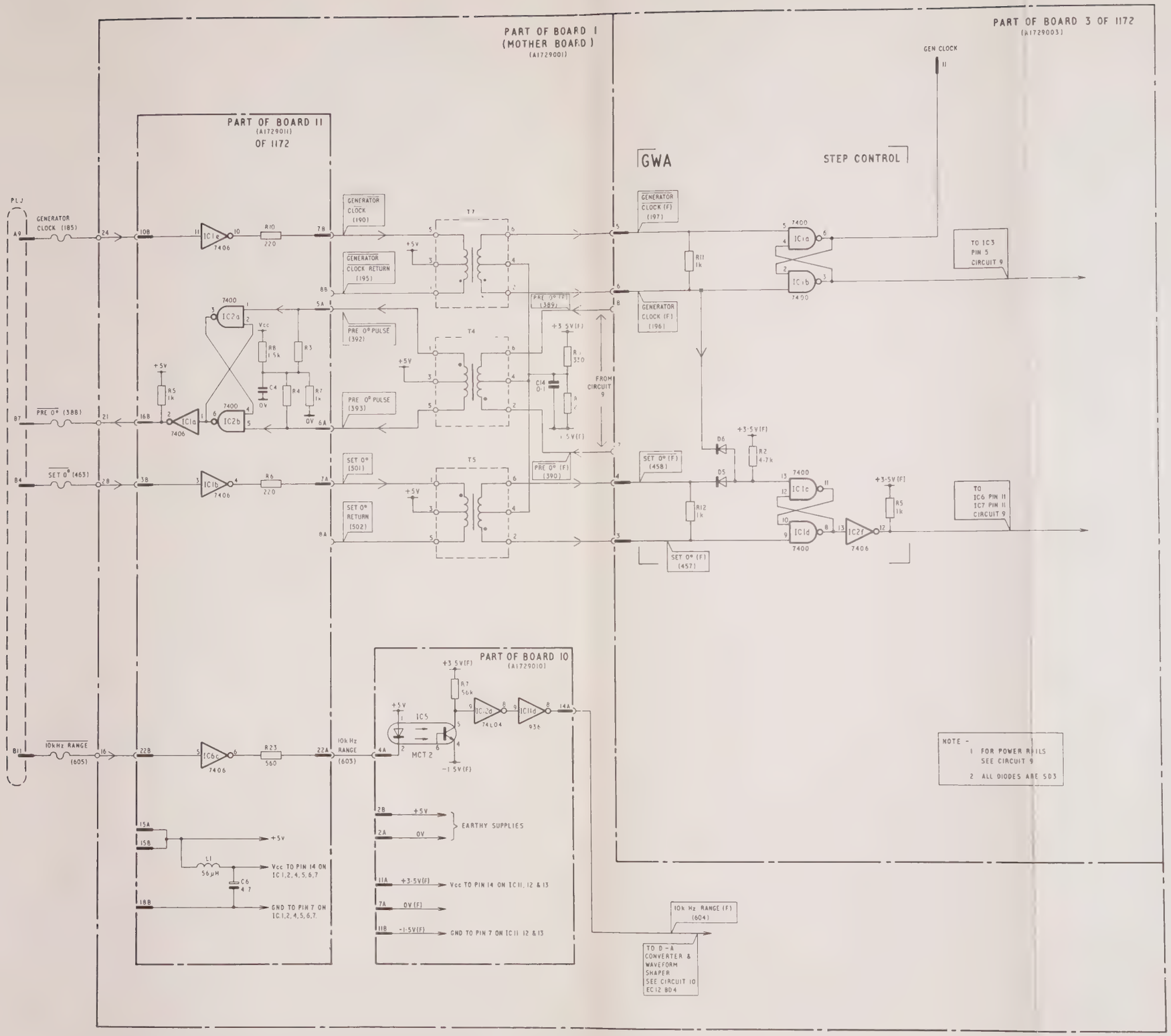
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 8

SOURCE	SIG No.	DESTINATION
50	605	
50	463	52
	388	50
50	185	52
	603	
	604	10
	190	
	195	
	392	
	393	
	501	
	502	
9	389	
9	390	
	197	
	196	
	458	
	457	



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 9 See page 1.3.12

The clock input IC3b pin 5 is at 2000f (or 200f) where f is the measurement frequency. The Rev counter outputs (439 to 448) carry a BCD count of the input clock. The counter counts 500 pulses per quadrant (or 50 in high frequency operation). The quadrant is defined by the waveform polarity outputs (389 and 390) and the set 0^{O} input to circuit 8.

Interconnections

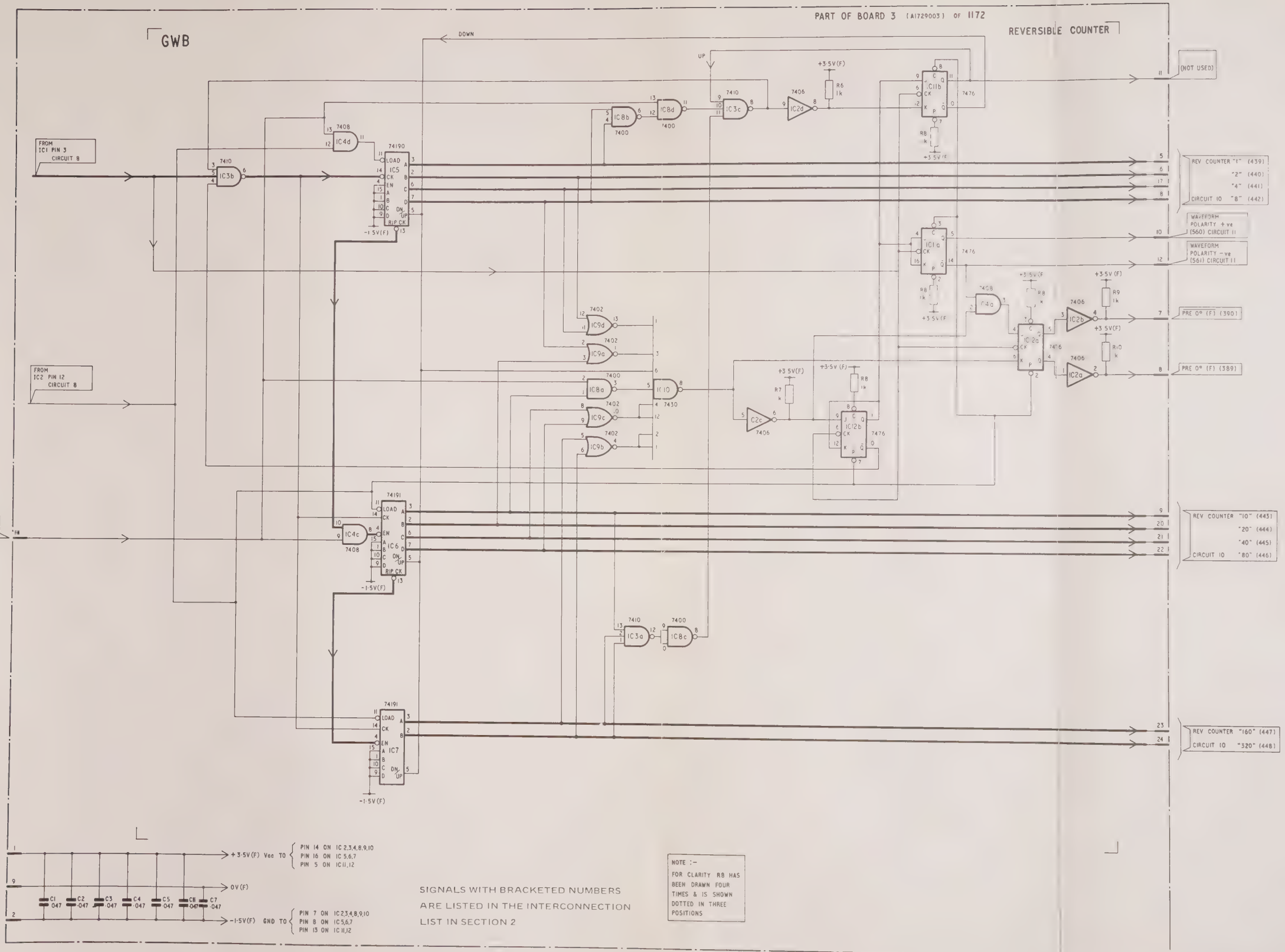
Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 9

SOURCE	SIG No.	DESTINATION
10	602	
	439	10
	440	10
	441	10
	442	10
	560	11
	561	11
	390	8
	389	8
	443	10
	444	10
	445	10
	446	10
	447	10
	448	10

GWB

REVERSIBLE COUNTER



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

NOTE :-
FOR CLARITY R8 HAS BEEN DRAWN FOUR TIMES & IS SHOWN DOTTED IN THREE POSITIONS

Circuit 10 See page 1.3.12

The 0–500–0 BCD count on inputs 439 to 448 produce a staircase triangular waveform at the summing junction to IC3 which is modified by the selectable waveform shaper to produce at the outputs (562 and 563) a square, sine or triangular waveform. Only two quadrants of the waveform are produced in this circuit, the other two quadrants being produced by polarity switching in circuit 11.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 10

SOURCE	SIG No.	DESTINATION
	602	9
9	448	
9	447	
8	604	
9	446	
9	445	
9	444	
9	443	
9	442	
9	441	
9	440	
9	439	
35	497	38
	498	
	499	
	198	13
	563	11
	562	11

PART OF BOARD I (MOTHER BOARD) (A1729001)

BOARD 4 OF 1172 (A1729004)

PART OF BOARD II (A1729011) OF 1172

PART OF BOARD 10 (A1729010) OF 1172

NOTE:-
1 FOR POWER RAILS ON BOARDS 10 & 11 SEE CIRCUIT 8
2 ALL DIODES SD3 UNLESS OTHERWISE STATED.

SINE (F) FROM PIN 15A – BOARD 10 (473) SEE CIRCUIT 14

GWC

MODE CONTROL

GWD REFERENCE

GWE

WAVEFORM SHAPER

GWF

D-A CONVERTER

GWG INVERTER

GENERATOR 10.6V REF (198) CIRCUIT 13

NOT USED

WAVEFORM -VE CIRCUIT 11 (563)

WAVEFORM +VE CIRCUIT 11 (562)

REV COUNTER "1" (439)
"2" (440)
"4" (441)
"8" (442)
"10" (443)
"20" (444)
"40" (445)
CIRCUIT 9 "80" (446)
10kHz RANGE (F) (604)

REV COUNTER "160" (447)
CIRCUIT 9 "320" (448)
10kHz RANGE (F) CIRCUIT 9 (602)

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 11 See page 1.3.12

The output selector is used to assemble the complete output waveform from the quadrants generated in circuit 10.

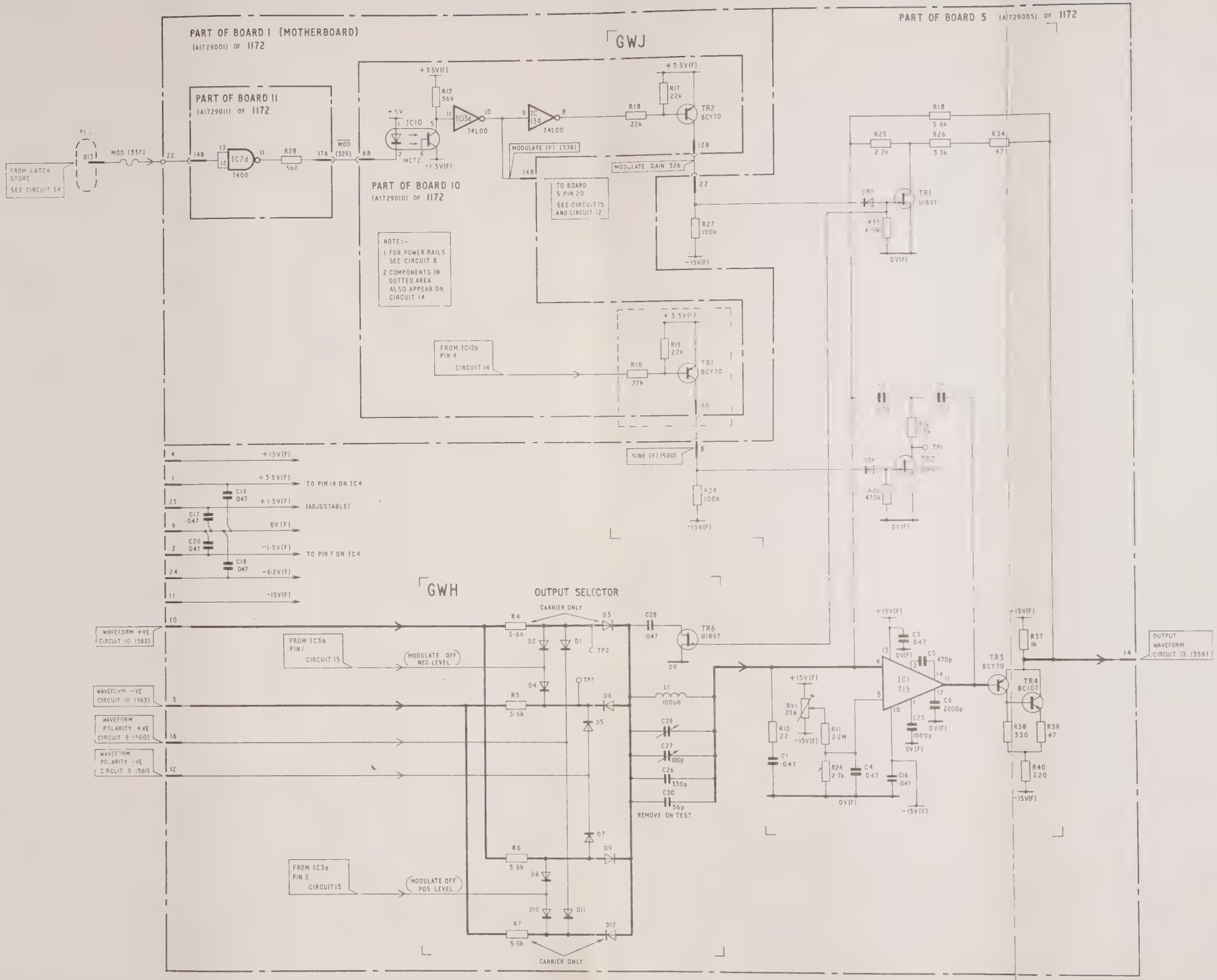
Block GWJ adjust the output amplitude by changing the gain of IC1 when sine or modulated outputs are selected. The output is modulated by the carrier waveform from circuit 15 to D4 and D8 anodes if MOD is selected.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 11

SOURCE	SIG No.	DESTINATION
9	561	
9	560	
10	563	
10	562	
34	337	41
	329	
	338	12.15
	326	
14	500	
	356	13



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 12 See page 1.3.12

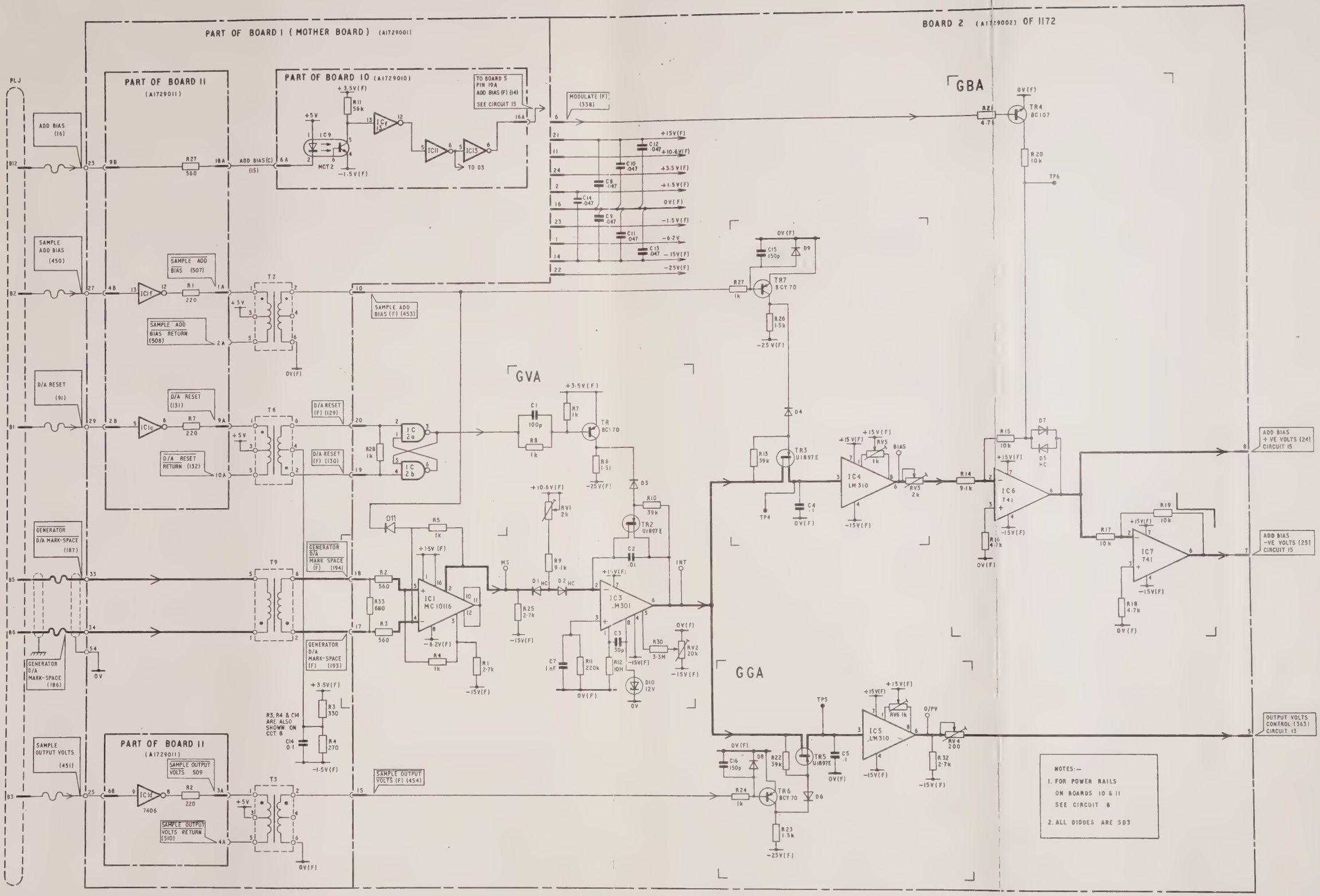
This circuit is used to provide voltage control for both the main and bias generators. The D/A mark/space signal is shared between the two generators by the sample and hold technique. See the generator block diagram for a description of the principle.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 12

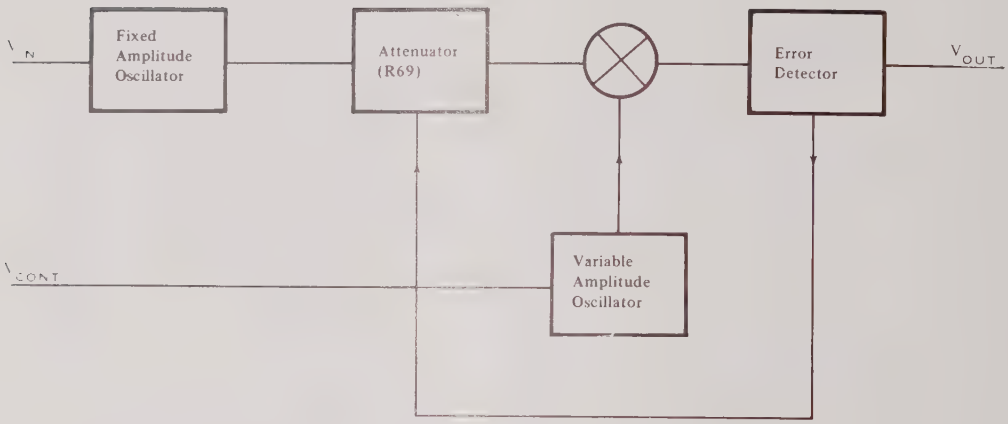
SOURCE	SIG No.	DESTINATION
72	451	
72	186	
72	187	
72	91	
72	450	
34	16	41
	24	15
	25	15
	363	13
	15	
	507	
	508	
	131	
	132	
	453	
	129	
	130	
	194	
	193	
	454	
	509	
	510	
11	338	15
	14	15



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 13 See page 1.3.12

This circuit is a programmable attenuator controlled by the analogue voltage from circuit 12 (363).



The input voltage has added to it an 800kHz fixed amplitude alternating voltage. After the signal current passes through the optically variable resistive attenuator it has the output of the variable oscillator added in antiphase with the fixed oscillator voltage. Any 800kHz left after this summation is detected in amplitude and phase by the error detector. By optical coupling the output of the error detector is used to increase or decrease the value of the attenuator.

The value of the attenuator is therefore proportional to the amplitude of the variable oscillator and hence of the control voltage V_{CONT}.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 13

SOURCE	SIG No.	DESTINATION
12	363	
10	198	
11	356	
	384	14

OUTPUT WAVEFORM CIRCUIT 11 (356)

GENERATOR 10 nV REF CIRCUIT 10 (198)

OUTPUT VOLTS CONTROL CIRCUIT 12 (363)

GAA

800 kHz OSCILLATOR

GAB

GAC

FILTER

GAD

800 kHz OSCILLATOR (VARIABLE AMPLITUDE)

GAE

ERROR DETECTOR

VARIABLE GAIN AMPLIFIER

PROGRAMMABLE ATTENUATOR OUTPUT (384) CIRCUIT 14

NOTE -
1 ALL TRANSFORMER CORES ARE CONNECTED TO 0V(F)
2 DENOTES HEAT SINK

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 14 See page 1.3.12

This circuit provides final amplification of the output voltage and attenuation for selected range by relays A to D.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 14

SOURCE	SIG No.	DESTINATION
3	359	
3	360	
13	384	
	354	
	352	
	351	
	353	
35	474	38
	472	
	473	10
	500	13
	365	
	88	
	687	
	362	

PART OF BOARD I (MOTHER BOARD) OF 1172
(AI729001)

BOARD 8 (AI729008) OF 1172

MAIN OUTPUT AMPLIFIER

GOA

PART OF BOARD II
(AI729011) OF 1172

PART OF BOARD IO OF 1172
(AI729010)

PART OF BOARD
14 (AI729014)

NOTE
1 FOR POWER RAILS ON BOARDS IO & II SEE CIRCUIT 8
2 ALL DIODES ARE SD3 UNLESS OTHERWISE STATED

PROGRAMMABLE ATTENUATOR OUTPUT (384) CIRCUIT 13

SINE (474)

SINE (473) CIRCUIT IO

+25V(F) +15V(F) +3·5V(F) TO PIN 14 ON IC2 0V(F) −1·5V(F) TO PIN 7 ON IC2 −5V.F) −25V(F)

IC1 LM301A

IC3 MC¹2

IC6a IC6b IC6c IC6d 7406

IC10a IC10b IC10c IC10d 74LO0

IC12a IC12b IC12c IC12d 74LO0

IC2 MCT2

IC4 IC5 IC7 IC8 74LO0

IC9a IC9b IC9c IC9d 7405

IC11a IC11b IC11c IC11d 7404

TR1 BCY70
TR2 2N2484
TR3 MM1613
TR4 MM1614
TR5 2N2484
TR7 2N4037
TR10 2N3053
TR11 BC107A
TR12 BC107A
TR13 U1897E

D1 D2 D3 D4 D5 D11 D12 D13 D14 D15

R1 820k
R2 9·1k
R3 1k
R4 3·9k
R5 1k
R6 680k
R7 47k
R8 56k
R9 220
R10 1k
R11 1k
R14 4·7k
R15 10
R16 10
R17 150
R18 330
R20 270
R21 470
R22 5·6k
R23 270
R24 560
R25 4·7k
R31 15k
R32 4·7k
R40 820
R43 100k
R45 4·7k
R47 1·5k
R48 470k
R49 10K
RV1 20k

C1 ·047
C2 ·047
C3 47p
C4 150p
C5 22
C7 100p
C8 22p
C9 22
C10 ·022
C11 390p
C12 390p
C14 ·1µ
C15 ·047

RLA(1) RLB(1) RLC(1) RLD(1)

OUTPUT (MAIN) (365)

OUTPUT

COMMON

FRONT PANEL

OUTPUT VOLTS EXPONENT 2 (360)
OUTPUT VOLTS EXPONENT 1 (359)
OUTPUT VOLTS EXPONENT 2 (352)
OUTPUT VOLTS EXPONENT 2 (F) (351)
OUTPUT VOLTS EXPONENT 1 (F) (353)
OUTPUT VOLTS EXPONENT 1 (354)

OUTPUT OVERLOAD (F) (362)

PART OF BOARD IO (AI729010)
(MAIN) OVERLOAD

NOTE — IC2 IS NOT NORMALLY FITTED

ACLASSIFIEC (647)

GOB

RANGE

GOC

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 15 See page 1.3.12

If bias is selected by input (14) the dc polarity or ac phase is selected by input (26).

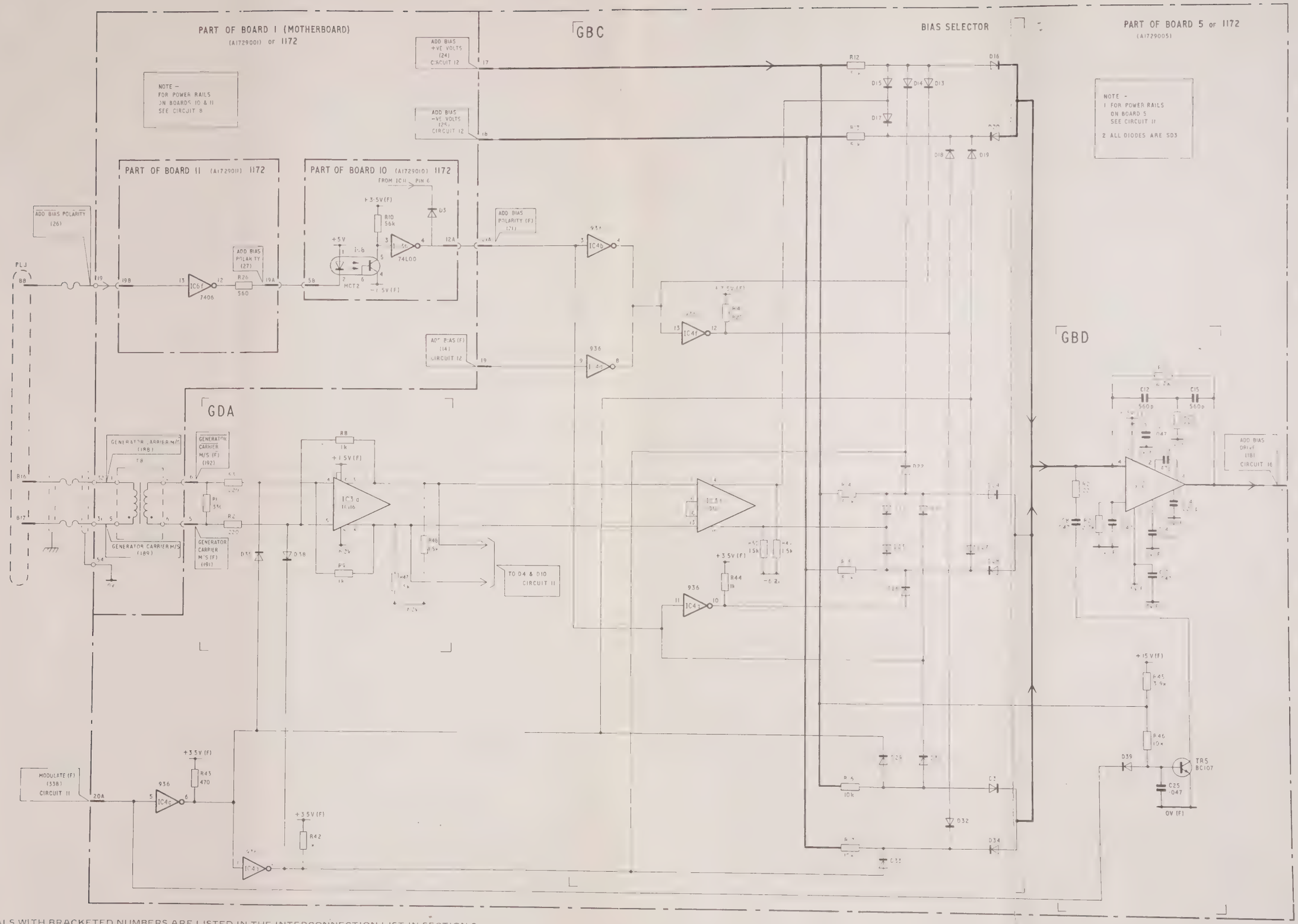
If modulate is selected by input (338) then a carrier waveform will be present in a mark/space form on inputs (189 and 189). The mark/space signal is used to convert the add bias + and – volts inputs (24 and 25) into an alternating voltage by the diode switching arrangement.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 15

SOURCE	SIG No.	DESTINATION
11	338	12
	189	
	188	
	191	
	192	
3	26	
	27	
12	24	
12	25	
	21	
12	14	
	18	16



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2.

1172 BIAS MODULATOR
D11707015 C

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 16

SOURCE	SIG No.	DESTINATION
15	18	
	364	
	88	
	686	
	47	

PART OF BOARD 1 (MOTHER BOARD) OF 1172
(A1729001)

BOARD 7 (A1729007)
OF 1172

GEA

BIAS OUTPUT AMPLIFIER

NOTE :-
1. FOR POWER RAILS ON BOARD 10 SEE CIRCUIT 8
2. ALL DIODES ARE 1S03 UNLESS OTHERWISE STATED

ADD BIAS DRIVE (18)
CIRCUIT 15

IC1 LM301A

TR1 BCY70
TR2 2N2484
TR3 MM1613
TR4 MM1614
TR5 2N2484
TR6 2N3053
TR7 2N4037
TR8 2N4037
TR9 2N3053
TR10 2N3053

D1 D2 D3 D4 D5 D6 D7 D8 D9 BAY72

RV1 20k
RV2 50

OUTPUT (BIAS) (1364)

NOTE :- FIT LKA FOR 10Ω OUTPUT IMPEDANCE

PART OF BOARD 14 (A1729014)

BIAS
COMMON
FRONT PANEL

+25V(F) +15V(F) 0V(F) -15V(F) -25V(F) +3·5V(F) -1·5V(F)

GEB

PART OF BOARD 10 (A1729010)
(BIAS) OVERLOAD

TR11 TR12 BC107A

7404

MCT2

NOTE :- IC1 IS NOT NORMALLY FITTED

UNCLASSIFIED (686)

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 17

SOURCE	SIG No.	DESTINATION
2	606	54.44
	631	13.14.16
	627	10.11.12.13.14.16
	625	11.12
	630	12.13.14.16
	626	10.11.12.13.14.16
	624	8.9.10.11.12.14.16
	623	11.12
	622	8.9.10.11.12.14.16

PART OF BOARD I (MOTHERBOARD) OF 1172
(A1729001)

PART OF BOARD II (A1729011) OF 1172

GIA INVERTER DRIVER

GIB INVERTER

BOARD 9 (A1729009) OF 1172

GPA +15V SUPPLY

GPB −6·2V SUPPLY

GPC −15V SUPPLY

GPD +1·5V SUPPLY

GPE −1·5V SUPPLY

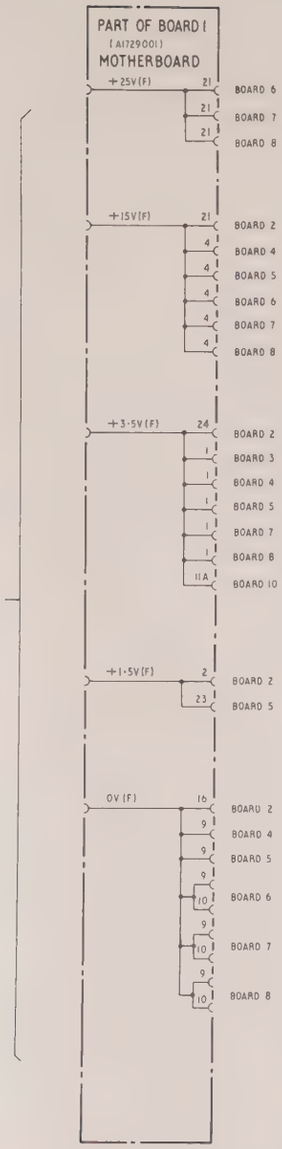
NOTE –
SUFFIX (F) DENOTES A FLOATING SUPPLY E.G. +25V(F) WHERE NO SUFFIX IS GIVEN THE SUPPLY IS REFERENCED TO EARTH

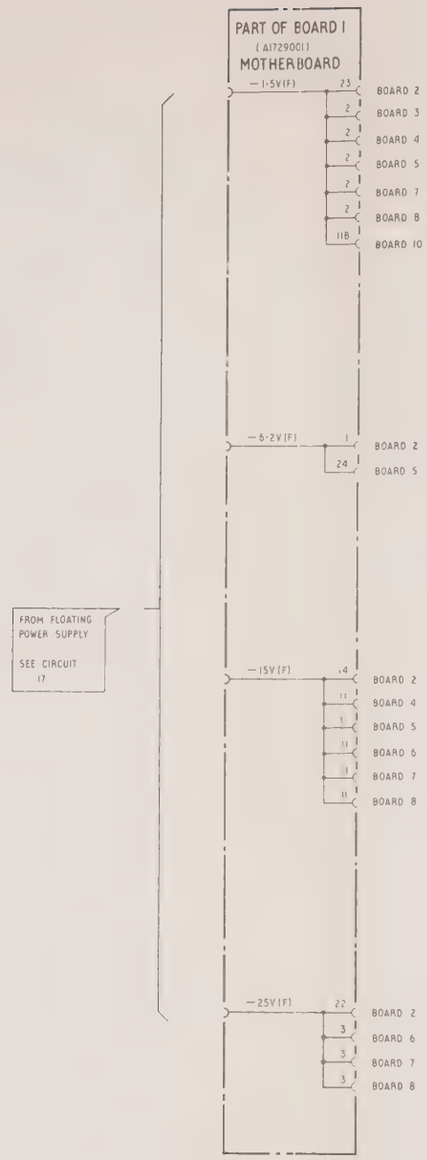
2 DENOTES HEAT SINK

3 ALL DIODES 5D3 UNLESS OTHERWISE STATED

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 18 See page 1.3.8





SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 19 See page 1.3.16

This circuit selects either the X or the Y input to be connected to circuit 20. The selection is made by input (571). When the selection is changed, a sequence of relays are selected in turn by the 100Hz clock (599) before settling on the appropriate selection. This is to ensure that any capacitive voltages are not transferred to the new input. The sequence is in five steps from X to Y or Y to X, the relays closing in the following order.

Step		Relays Mode (X = Closed)						
		A	B	C	D	E	F	G
(Y selected)	0	X	X				X	X
	1						X	
	2			X		X	X	
	3			X		X		
	4			X	X	X		
(X selected)	0			X	X	X		X
	1			X				
	2		X	X			X	
	3		X				X	
	4	X	X				X	X
(Y selected)	0	X	X				X	X

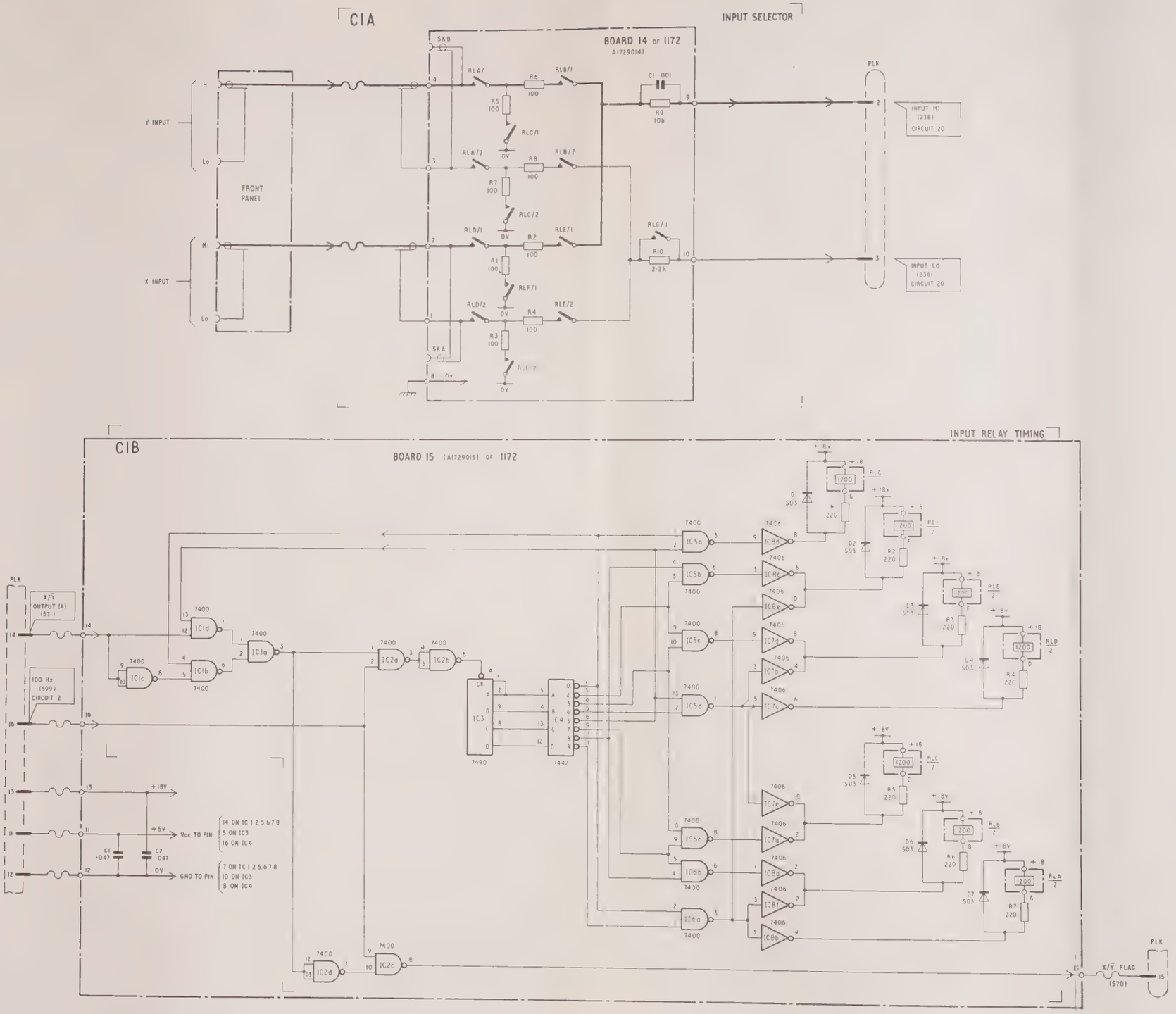
When the sequence is finished and the selection made, the output (570) changes.

Interconnections

Signal numbers are as in Section 2.4
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 19

SOURCE	SIG No.	DESTINATION
2	599	50 54
62	571	
	570	64
	238	20
24	236	20



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 20 See page 1.3.16

A two stage attenuator and amplifier circuit. The first stage is a switched attenuator of X1, X.01 or X.001 followed by an amplifier of X10 (no bias reject). The second stage is a switched attenuator of X1 or X0.1 followed by an amplifier of X10 (normal).

Range selection is as follows:-

	1st Atten.	2nd Atten.	Overall gain
10mV	X1	X1	100
100mV	X1	X0.1	10
1V	X.01	X1	1
10V	X.01	X0.1	0.1
100V	X.001	X0.1	.01

In addition the first amplifier gain is varied by the bias reject input (418). This is a variable voltage from the bias reject circuit, No. 24.

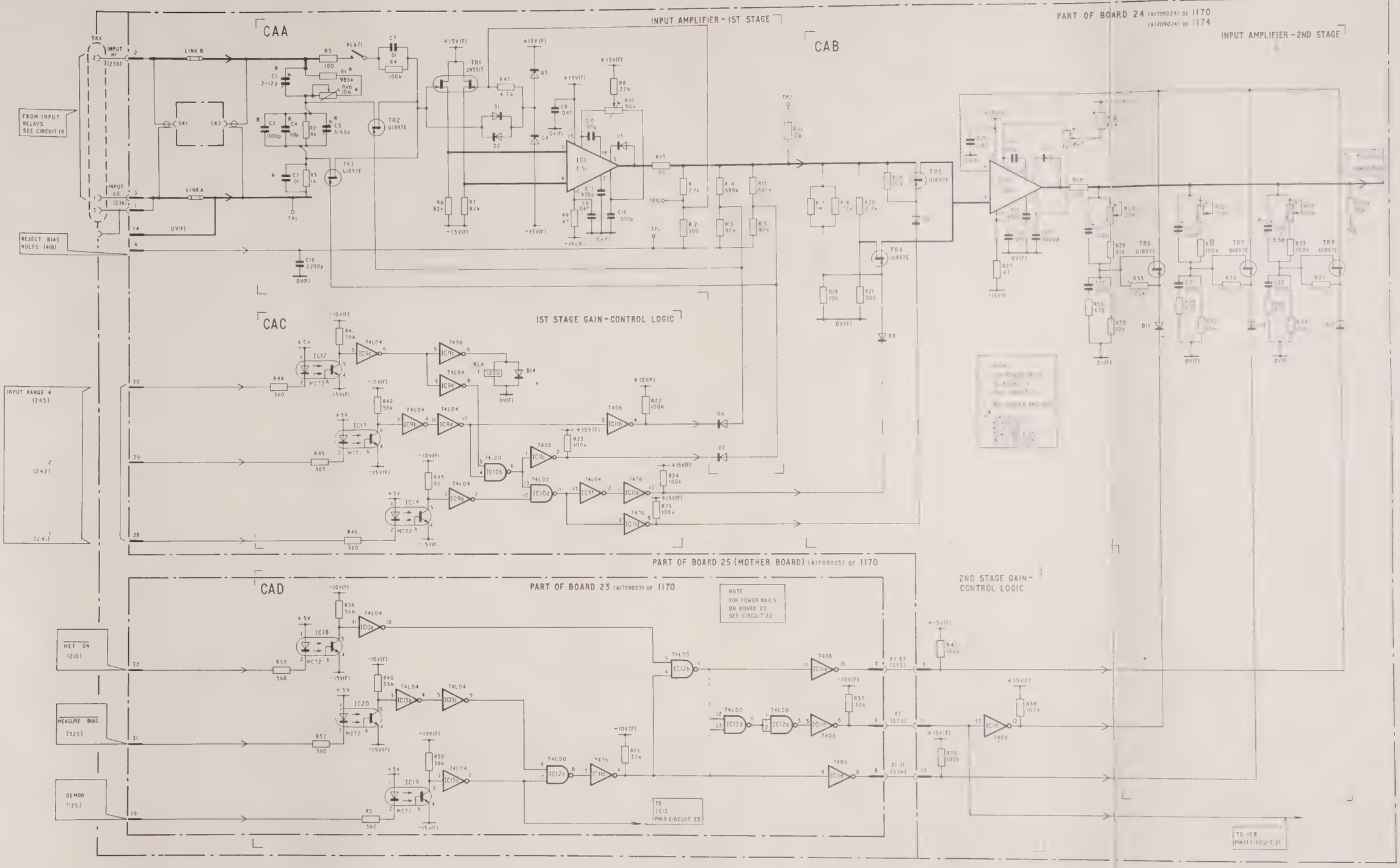
The second amplifier gain is altered from X10 to X11 or X16 depending on the selections of inputs (210), (323) and (125).

Interconnections

Signal numbers are as in Section 2.4
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 20

SOURCE	SIG No.	DESTINATION
34	125	52
62	323	50 52.56
50	210	52
73	241	65
73	242	63
73	243	3
24	418	
19.24	236	
19	238	
	575	
	573	
	574	



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 21 See page 1.3.16

The principle of the demodulator is shown in the block diagram for the input system. If Heterodyne, demodulate or measure bias mode is in operation the connection from circuit 20 (573) enables the chop input (66). This will chop the main signal at a frequency as explained in the block diagram.

The V to f converter is also explained in the block diagram.

The input overload output is used to operate the autorange system as well as to indicate overload.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 21

SOURCE	SIG No.	DESTINATION
2	611	25.50.54.58.65.66.69.70.72.
52	66	
20	573	
22	83	
	555	54
	260	73

CVA

CVB

CDA

DEMODULATOR

CVC

CAE

OVERLOAD DETECTOR

FROM R28 CIRCUIT 20

FROM EC11 (S73) CIRCUIT 20

2MHz (61)

2MHz

+5V FROM EC22

-10V(F)

+15V(F)

-15V(F)

0V(F)

-5V(F)

+10.6V REFERENCE

INPUT OVERLOAD (2601)

+5V Vcc TO PIN 14 ON IC15

0V GND TO PIN 7 ON IC15

EARTHY SUPPLIES

+15V(F)

0V(F) Vcc TO PIN 14 ON IC6 PIN 5 ON IC7

-5V(F) GND TO PIN 7 ON IC6 PIN 13 ON IC7

-10V(F) Vcc TO PIN 14 ON IC 8 9 10 11

-15V(F) GND TO PIN 7 ON IC 8 9 10 11

FLOATING SUPPLIES

NOTE
ALL DIODES SD3
UNLESS OTHERWISE
STATED

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 22 See page 1.3.16

This circuit generates an analogue dc voltage, used to back-off the bias, by means of a digital signal with a variable mark-to-space ratio. The input to IC7 is proportional to the mean level of the variable mark/space input (419/417). The output of IC7 ramps up when enabled by the reset logic, controlled from input (425/426). The ramp slope is proportional to the mark/space ratio.

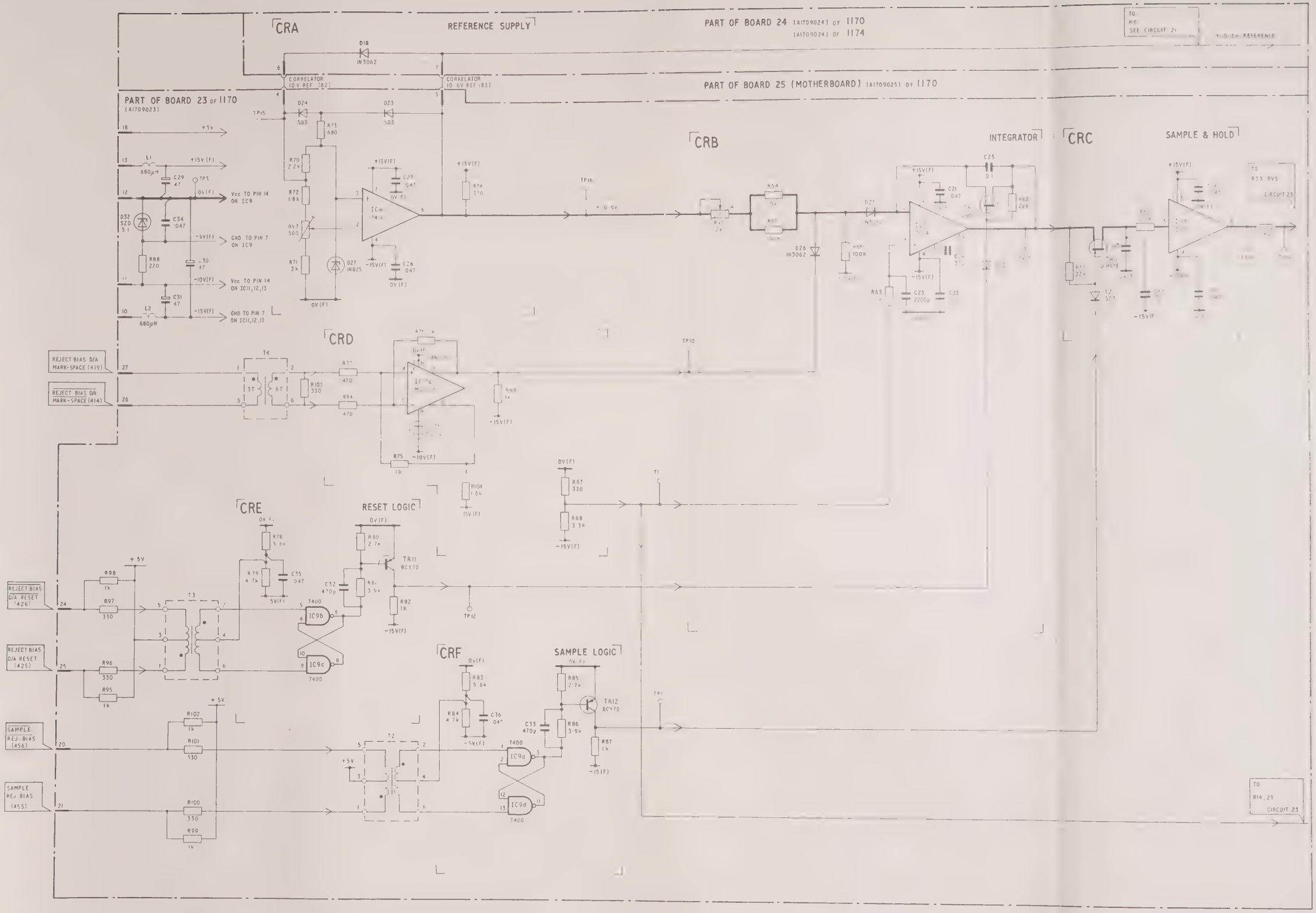
After a certain time the sample command will be given from input (455/456). The sampled ramp voltage will be held on the output of IC6 and updated periodically.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 22

SOURCE	SIG No.	DESTINATION
72	455	
72	456	
72	425	
72	426	
72	414	
72	419	
	82	
	83	21



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 23 See page 1.3.16

The dc voltage from circuit 22 is selected for polarity by block CMD from input (417). In the case of non-carrier mode this is a + or − decision.

If carrier mode is in operation demod will be called and blocks CME and CMC will be operative. In this case the mark/space representation of the carrier wave on inputs (61/62) will be used to modulate the voltage from circuit 22 in block CMA to provide an ac output at the carrier frequency. The phase will be determined by the bias reject decision in block CMD.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 23

SOURCE	SIG No.	DESTINATION
	61	
	62	
69	417	

PART OF BOARD 23 OF 1170
(AI709023)

CRG

CMA

CMB

CMC

CMD

CME

FROM IC6 PIN 6 CIRCUIT 22

FROM TP 18 & 19 CIRCUIT 22

FROM R67,68 CIRCUIT 22

FROM TP17 CIRCUIT 22

FROM IC13 PIN 2 CIRCUIT 20

DC OR AC BIAS VOLTAGE TO BIAS AMPLIFIER SEE CIRCUIT 24 R7 & TR1 CIRCUIT 24

REJ BIAS POLARITY (417)

CORRELATOR CARRIER MARK-SPACE (62)

CORRELATOR CARRIER MARK-SPACE (61)

NOTE -
1. FOR POWER RAILS SEE CIRCUIT 22
2. ALL DIODES SD3 UNLESS OTHERWISE STATED

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 24 See page 1.3.16

The value of the bias reject voltage is determined by this selectable gain amplifier.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers;
if none shown all connections are within this circuit.

CIRCUIT No. 24

SOURCE	SIG No.	DESTINATION
63	50	
63	51	
	418	20
	236	19.20

NOTE:-
FOR POWER RAILS
SEE CIRCUIT 22

CBA

BIAS AMPLIFIER

FROM IC2
PIN 11
CIRCUIT 23

FROM TP2 ON DRG 23

+15V(F)
C1 ·047 0V(F)
C3 ·001
RV1 1k
R5 1·5k
R6 1·5k
IC1 310
R89 470k
C4 220
−15V(F)
C2 ·047
R92 100
TP1
REJECT BIAS VOLTS (418)

TR1 2N4303
R7 2·7k
R1 22k
TR2 2N4303
R8 270
R2 22k
TR3 2N4303
R3 22k
R9 33
R10 330
R4 22k
TR4 2N4303

OV FROM BOARD 24
R91 10
0V(F)
INPUT LO (236)

CBB

BIAS RANGE DECODE

−10V(F)
R42 56k
+5V
IC22
IC16b
74L04
MCT2
−15V(F)
BIAS RANGE B (51)
30
R54 560

−10V(F)
R41 56k
+5V
IC21
IC16a
MCT2
−15V(F)
BIAS RANGE A (50)
29
R53 560

IC16e
IC16f

74L00 IC15
7406 IC14

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 25 See page 1.3.22

The Strobe Generator (block FGA) generates a 0.5μs pulse at a prf of 500kHz. They are steered to each of 16 outputs in turn by IC25 and IC15, but only the outputs shown are used. Each output will receive 16 pulses in a complete sequence of 256 counted by the binary down counter (block FCC).

The outputs $\overline{16}$ to $\overline{128}$ are used in circuit 29 to serialise data.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 25

SOURCE	SIG No.	DESTINATION
72	174	30
2	611	21.50.54.58.65.66.69.70.72

PART OF BOARD 16 OF PLUG-IN
(A1729016)

NOTE -
1 FOR POWER RAILS SEE CIRCUIT 38
2 —● DENOTES FLEXSTRIP CONNECTOR
—○ DENOTES TERMINAL PIN
(SEE CIRCUIT 38)

FCA DIVIDE BY FOUR

FCB BUFFER

FCC BINARY DOWN COUNTER

FGA STROBE GENERATOR

2MHz (611) CIRCUIT 2

PL1

CLOCK FROM BOARD 17 PIN 6 CIRCUIT 30

FRONT PANEL SYNC (174)

TO PCB17 PIN 5 CIRCUIT 30

500 kHz

TO IC29 PINS 1, 4, 5 CIRCUIT 26

TO SERIALISER SEE CIRCUIT 29

TO INTEGRATION TIME TOUCH KEY LATCHES SEE CIRCUIT 40

TO MEASUREMENT DELAY TOUCH KEY LATCHES SEE CIRCUIT 40

TO DISPLAY TOUCH KEY LATCHES SEE CIRCUIT 39

TO MODE TOUCH KEY LATCHES SEE CIRCUIT 39

TO MEASUREMENT TOUCH KEY LATCHES SEE CIRCUIT 39

TO INPUT RANGE TOUCH KEY LATCHES SEE CIRCUIT 40

TO AUTO RANGE TOUCH KEY LATCH SEE CIRCUIT 40

TO SWEEP COMMAND TOUCH KEY LATCHES SEE CIRCUIT 39

TO SWEEP MODE TOUCH KEY LATCH SEE CIRCUIT 38

TO KEYBOARD FUNCTION TOUCH KEY LATCHES SEE CIRCUIT 38

TO CARRIER TOUCH KEY LATCH SEE CIRCUIT 41

TO BIAS TOUCH KEY LATCH SEE CIRCUIT 41

TO CONTROL TOUCH KEY LATCH SEE CIRCUIT 41

TO IC33 PIN 9 CIRCUIT 29

TO BOARD 16 CIRCUIT 29

STROBES TO TOUCH KEYS SEE CIRCUIT 26

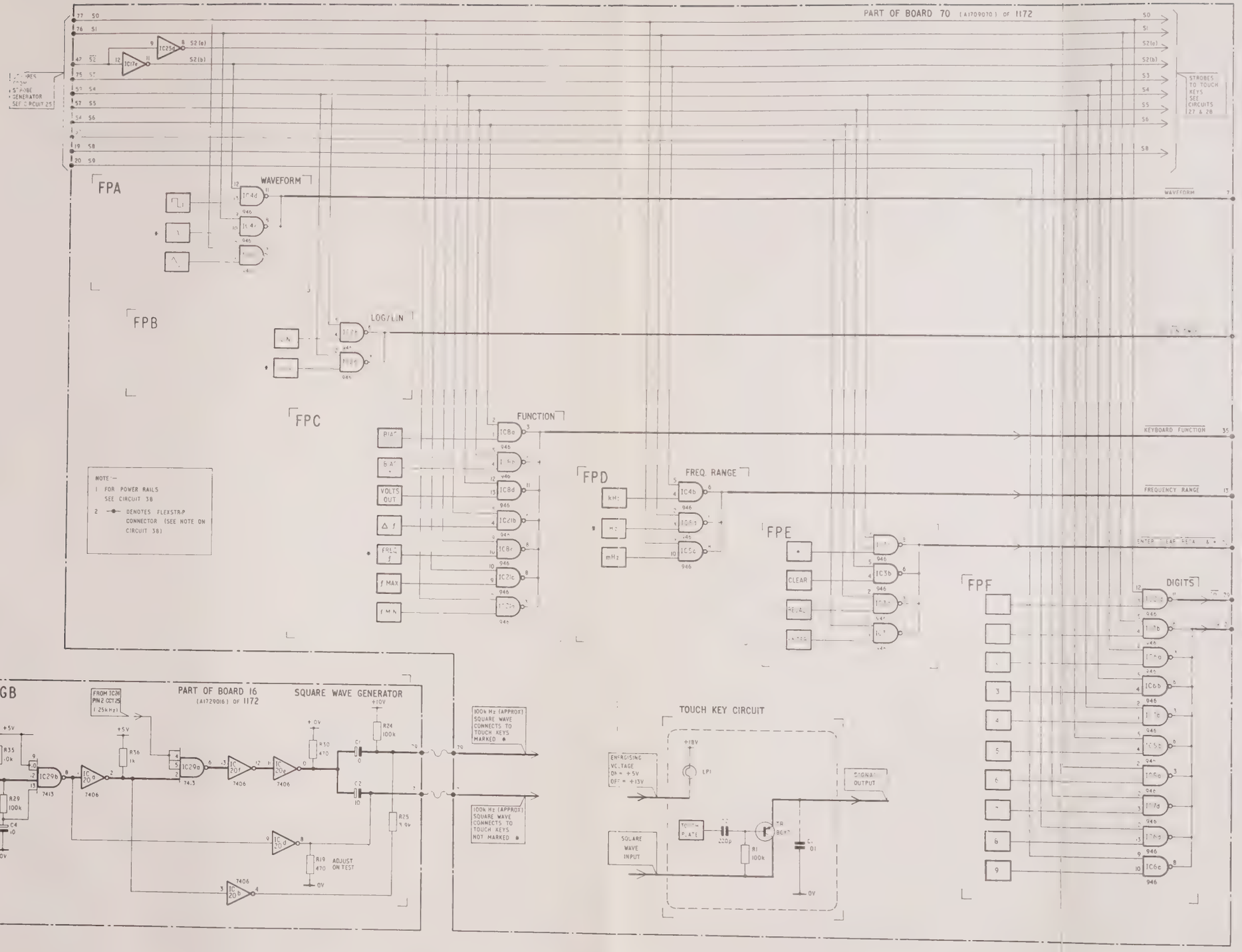
NOTE
THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 26 See page 1.3.22

CIRCUITS 26 to 28

When a touch key is touched the output goes high. The appropriate output to circuit No. 29 will therefore go high during the particular strobe pulse.


PART OF BOARD 70 (A1709070) OF 1172
FPA
WAVEFORM
FPB
LOG/LIN
FPC
FUNCTION
FPD
FREQ. RANGE
FPE
FPF
DIGITS
KEYBOARD FUNCTION
FREQUENCY RANGE
STROBES TO TOUCH KEYS SEE CIRCUITS 27 & 28
SEE CIRCUIT 29
NOTE
THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS
NOTE —
1 FOR POWER RAILS SEE CIRCUIT 38
2 DENOTES FLEXSTRIP CONNECTOR (SEE NOTE ON CIRCUIT 38)
FGB
PART OF BOARD 16 (A1729016) OF 1172
SQUARE WAVE GENERATOR
FROM IC3d PIN 2 OCT 25 (1.25kHz)
FROM SYNC MAIN SET LOGIC SEE CIRCUIT 30
100k Hz (APPROX) SQUARE WAVE CONNECTS TO TOUCH KEYS MARKED *
100k Hz (APPROX) SQUARE WAVE CONNECTS TO TOUCH KEYS NOT MARKED *
ADJUST ON TEST
TOUCH KEY CIRCUIT
ENERGISING VOLTAGE ON = +5V OFF = +13V
SQUARE WAVE INPUT
SIGNAL OUTPUT

Circuit 27 See page 1.3.22

CIRCUITS 26 to 28

When a touch key is touched the output goes high. The appropriate output to circuit No. 29 will therefore go high during the particular strobe pulse.

FROM STROBE GENERATOR SEE CIRCUIT 25

S0
S1
S2(a)
S2(b)
S3

FPG

MODE

* X
Y/X
Y

IC19c 946
IC19d 946
IC11d 946

$\overline{\text{MODE}}$ 55

FPH

MEASUREMENT

RECYCLE
* STOP
SINGLE

IC11a 946
IC11b 946
IC11c 946

$\overline{\text{MEASUREMENT}}$ 52

FPJ

DISPLAY

J b
* R θ
LOG R θ

IC24c 946
IC24b 946
IC25a 946

$\overline{\text{DISPLAY}}$ 69

TO SERIALISER SEE CIRCUIT 29

NOTE
THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS

NOTE:—
1 FOR POWER RAILS SEE CIRCUIT 38
2 SEE CIRCUIT 26 FOR INTERNAL CIRCUITRY OF INDIVIDUAL TOUCH KEYS AND FOR AN EXPLANATION OF KEYS MARKED *

FPK

SWEEP COMMAND

* OFF
HOLD
↑
↓

IC1a 946
IC1d 946
IC1c 946
IC1b 946

$\overline{\text{SWEEP COMMAND}}$ 8

FPL

CONTROL

REMOTE
* LOCAL

IC25b 946
IC25a 946

$\overline{\text{REMOTE}}$ 64
$\overline{\text{LOCAL}}$ 63

Circuit 28 See page 1.3.22

CIRCUITS 26 to 28

When a touch key is touched the output goes high. The appropriate output to circuit No. 29 will therefore go high during the particular strobe pulse.

FROM STROBE GENERATOR
SEE CIRCUIT 25

S0
S1
S2(a)
S3
S4
S5
S6
S8

FPM

INTEGRATION TIME

* MIN
X10
X100
X1000

946 IC15d
946 IC15b
946 IC14d
946 IC14b

INTEGRATION TIME 74

FPN

MEASUREMENT DELAY

* 1
1
10
100

946 IC15c
946 IC15a
946 IC14c
946 IC14a

MEASUREMENT DELAY 78

FPO

INPUT RANGE

100V
10V
1V
100mV
10mV
* AUTO RANGE

946 IC19a
946 IC20d
946 IC20b
946 IC19b
946 IC20a
946 IC20c

INPUT RANGE 56

TO SERIALISER
SEE CIRCUIT 29

NOTE
THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS

NOTE –
1. FOR POWER RAILS SEE CIRCUIT 38
2 SEE CIRCUIT 26 FOR INTERNAL CIRCUITRY OF INDIVIDUAL TOUCH KEYS AND FOR EXPLANATION OF KEYS MARKED *

FPP

CARRIER & BIAS

DEMOD INPUT
MOD OUTPUT
INPUT REJECT
OUTPUT ADD

946 IC17c
946 IC7c
946 IC17b
946 IC17a

DEMOD INPUT 41
MOD OUTPUT 38
INPUT REJECT 27
OUTPUT ADD 28

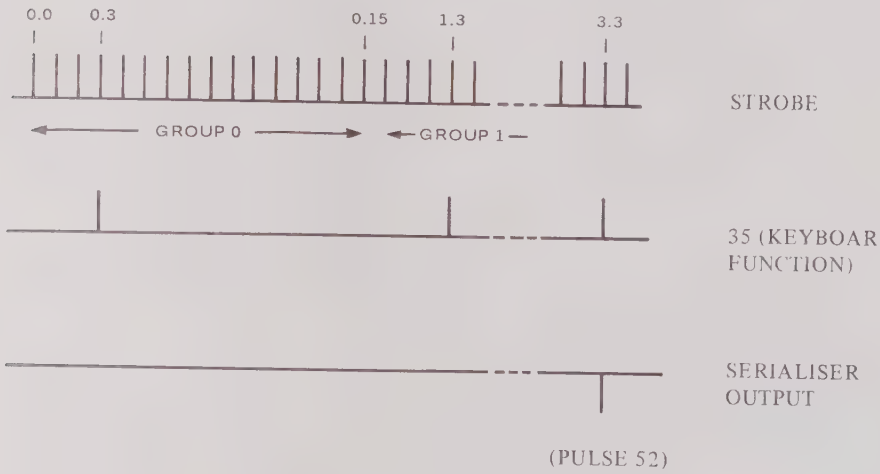
Circuit 29 See page 1.3.22

Each output of circuits 25 - 28 is examined in turn by IC's 17 and 3. A particular touch key is identified by a low pulse at the output in one of 256 time slots of 2μs.

Example, See Figure Below

Consider that touch key Δ f has been touched. The $\overline{\text{keyboard function}}$ (pin 35) line will go high for each strobe No. 3.

Each input to IC's 17 and 3 is examined for a period equal to 16 strobe pulses. The output will therefore go low for the period of strobe 3 of group 3. This is in fact the 52nd of the 256 time slots.



Interconnections Signal numbers are as in Section 2.4. Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.		
CIRCUIT No. 29		
SOURCE	SIG No.	DESTINATION
62	438	33.73

NOTE :-
1 FOR POWER RAILS SEE CIRCUIT 38
2. DENOTES FLEX STRIP CONNECTOR (SEE NOTE ON CIRCUIT 38)
DENOTES TERMINAL PIN

FSA SERIALISER 1 CONTROL

FSB SERIALISER 1

FSC SERIALISER 2

FSD SERIALISER OUTPUTS CONTROL

FROM IC37 PIN 6 CIRCUIT 41

LOCAL

$\overline{50}$

FROM IC25 PIN 9 CIRCUIT 25

+5V

R26 630

IC33e 7404

IC13a 7410

IC32d 7401

IC13b 7410

IC33f 7404

R11 1k R20 1k R17 1k R7 1k R18 1k R8 1k R16 1k R5 1k

MEASUREMENT 52
DISPLAY 69
INTEGRATION TIME 74
KEYBOARD FUNCTION 35
REMOTE 64
LOCAL 63
0 29
1-9 21

IC7f 7404 IC10e 7404 IC10a 7404 IC4c 7404 IC10f 7404 IC10c 7404 IC4d 7404 IC2e 7404

IC17 74 S1

PARALLEL DATA FROM TOUCH KEYS SEE CIRCUITS 26,27 & 28

NOTE
THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS

FROM BOARD 16 CIRCUIT 25

$\overline{16}$ 32 $\overline{64}$ $\overline{128}$

IC22b 862 IC22a 862 IC32c 7404 IC32a 7401

R27 680 IC33d 7404

IC34d 7401

+5v R28 680 IC33b 7404

SERIALISED DATA FROM TOUCH KEYS TO PULSE SHAPER TO PIN 4 OF BOARD 17 CIRCUIT 30

PLJ D16 RUN (438) 16

FROM IC32 PIN 4 CIRCUIT 25

R3 1k R4 1k R1 1k R9 1k R2 1k R6 1k R13 1k R10 1k

LOG, LIN SWEEP 12
SWEEP COMMANDS 8
BIAS-INPUT REJECT 27
FREQUENCY RANGE 13
ENTER, CLEAR, RECALL & • 22
WAVEFORM 7
BIAS - OUTPUT ADD 28
INPUT RANGE 56
MOD OUTPUT 38
MODE 55
DEMOD INPUT 41
MEASUREMENT DELAY 78

IC2c 7404 IC2b 7404 IC2a 7404 IC2f 7404 IC2d 7404 IC7a 7404 IC14c 7404 IC7c 7404

IC3 74151

IC34c 7401

PARALLEL DATA FROM TOUCH KEYS SEE CIRCUITS 26 27 & 28

NOTE:
THESE TITLES ARE NOT INCLUDED IN THE LIST OF 1170 SERIES INTERCONNECTIONS

Circuit 30 See page 1.3.22

This circuit shapes the serial data for transmission to the 1170.

The click relay provides an audible indication that a front panel selection has been activated.

The mains set input sets all latch store data to a state equivalent to that required at power "switch-on".

Monostable IC5a ensures that once a serial data pulse has been detected any others are inhibited for its period.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 30

SOURCE	SIG No.	DESTINATION
72	174	25
4	321	34.50.58.66
69	608	
	164	31

PART OF BOARD 17
(A1729017)
OF PLUG IN

FOA

1μS PULSE CHECKING LOGIC

SERIALISED DATA FROM TOUCH KEYS PIN 4 OF BOARD 16 CIRCUIT 29

IC4a 7413

IC6a 7474

IC6b 7474

IC3b 846

IC5a 74123

+5V R3 47k C3 10 D3 SD3 0V

7406 IC2e

7406 IC2d

7406 IC2f

+5V R5 680

IC3c

PL J 04

FP SERIAL O/P (164) CIRCUIT 31

FOB CLOCK INHIBIT

PL J D6

500kHz (608)

IC1a 74132

IC1b 74132

500kHz

CLOCK TO BOARD 70 PIN 6 CIRCUIT 25

+13V R6 33

+10V TR1 D1

+5V Vcc TO PIN 14 ON ICs 1,2,3,4,6 & PIN 16 ON IC5

C5 .047

0V GND TO PIN 7 ON ICs 1,2,3,4,6 & PIN 8 ON IC5

FOC SYNCHRONISED MAINS SET-DELAY

IC4b 7413

IC3d 846

D5 SD3 R2 100 R7 100k C2 15 0V

FOD CLICK RELAY

+5V R4 39k C4 D4 SD3

IC5b 74123

7406 IC2a IC2b

RLA 185 +13V D2 SD3

SYNCHRONISE MAINS SET

FOE

MAINS SET (321)

74132 IC1c IC1d

7406 IC2c

+5V R1 1k

FRONT PANEL SYNC (174)

TO PCB 16 PIN 5 CIRCUIT 25

TO BOARD 16 PIN 17 CIRCUIT 26

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 31 See page 1.3.22

This circuit controls the writing-in and reading of data in the latch store (circuit 32 to 36). The same 256 bit timing sequence is carried on lines T1 to T8 (530 to 537) as is used in circuit 25.

The 256 time slots are divided into 16 groups of 16. During each group, 16 Write and 16 Read strobes are generated at the same time as the data (from block FLA) increases in BCD from 0 to 15. Each output of block FMA is examined for the period of 1 group of 16 strobes. If a data pulse is received it will cause that particular output to change for the period of the particular time slot.

A particular bit of serial data will therefore coincide with a unique combination of outputs from blocks FMA, FWA and FLA, causing that particular bit to be written into the correct store location.

Numerical data from the keyboard are not stored in the Latch stores on pcb 14 but are passed directly into pcb 15 (circuit No. 70) via outputs (591/592).

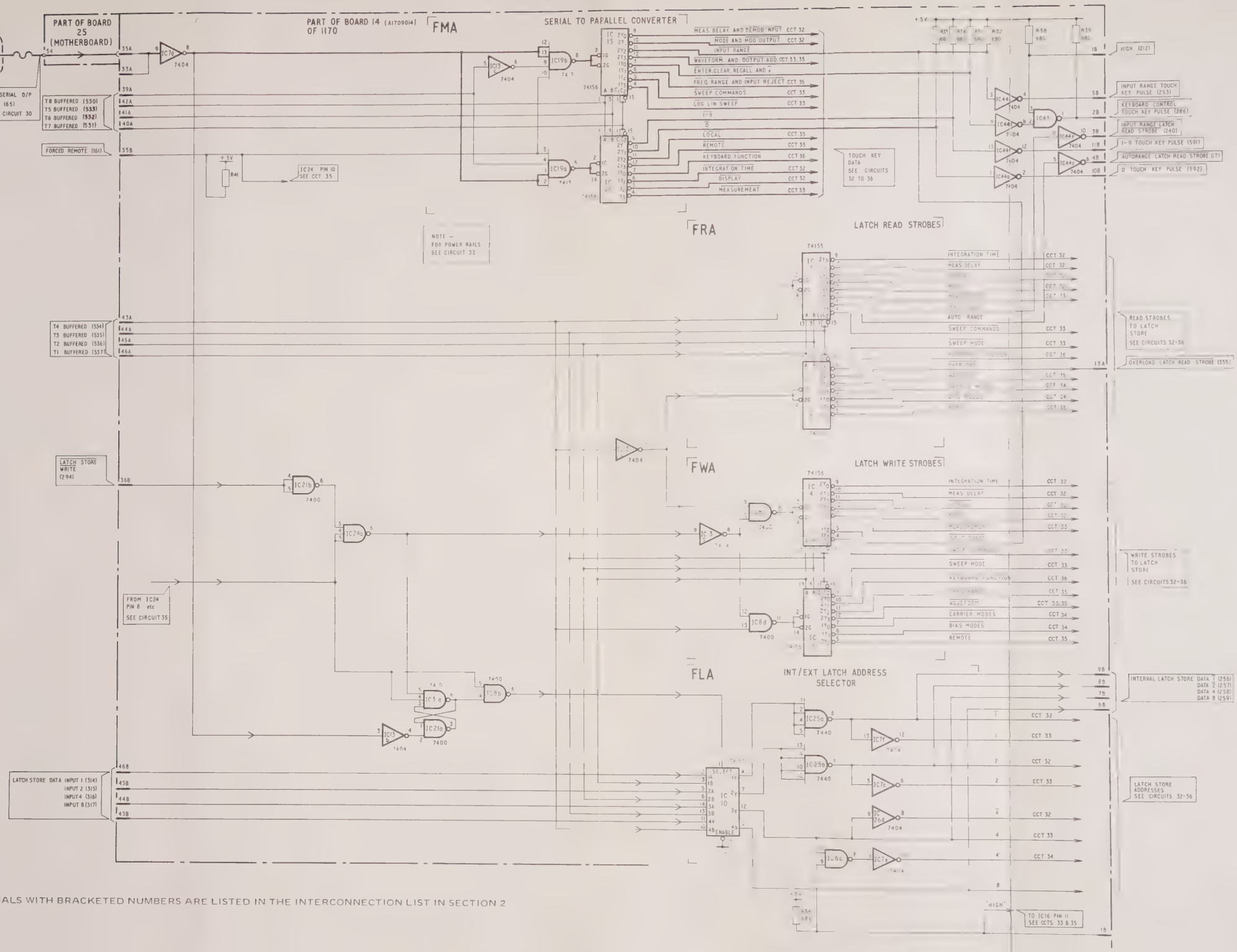
Autorange command is passed to pcb No. 17 (circuit No. 73). Input range data are held on IC30 on pcb No. 17 (circuit No. 73).

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. **31**

SOURCE	SIG No.	DESTINATION
	317	
	316	
	315	
	314	
	294	
69	537	
69	536	
69	535	
69	534	
	161	35
69	531	
69	532	
69	533	
69	530	
30	164	
	165	
	212	36.70.71
	253	73
	286	70
	240	73
	591	70
	17	73
	592	70
	355	73
	256	36.70.71.73
	257	36.70.71.73
	258	36.70.71.73
	259	70.73



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

CIRCUITS 32 to 36

The storage devices used to hold the front panel selections are "D" type flip flops.

Data are written - in by a clock pulse which is formed by a combination of a write strobe and a data pulse. The data that is written is generated in block FLA of circuit No. 31 (D inputs to the flip-flops).

The store locations are best understood if the instructions for the use of the Store State Indicator are referred to. Table 2 of the SSI lists the Latch Store locations. The following table relates this information to the hardware.

Contents of the stores are read in sequence by the read strobes generated in block FRA of circuit 31.

Store Location	Function	Circuit No	Block	PCB	IC
0 - 0	Integration time	32	FLB	14	34
0 - 1	Measure delay	32	FLC	14	34
0 - 2	Display	32	FLD	14	29
0 - 3	Measurement	32	FLE	14	29
0 - 4	Measure Sequence	33	FLF	14	36
0 - 5	Input Range	73		17	30
0 - 6	Input Range	73		17	30
0 - 7	Sweep Command	33	FLG	14	32
1 - 0	Sweep Mode	33	FLH	14	39
1 - 1	Keyboard	36	FLO	16	36
1 - 2	Frequency Range	35	FLM	14	42
1 - 3	Generator Mode	35	FLL	14	42
1 - 4	Carrier Mode	34	FLJ	14	11
1 - 5	Bias Mode	34	FLK	14	22
1 - 6	Control	35	FLN	14	24

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 32

SOURCE	SIG No.	DESTINATION
	247	50
	248	50
	324	50
	325	50
	128	69.71.74
	127	69.71
	347	64.69.71
	348	64.69.71

PART OF BOARD 14 OF 1170
(A1709014)

30A
30B
31A
31B
27A
27B
28A
28B

+5V
C1 .047
C2 .047
C4 .047
0V

Vcc TO PIN 14 ON ICs 1,2,6,7,8,11, 12,13,16,17,18,19,21-28, 30-33,35-41,43,44 & PIN 16 ON ICs 3-5,9,10, 15,20,29,34,42.

GND. TO PIN 7 ON ICs 1,2,6,7,8,11, 12,13,16,17,18,19,21-28 30-33,35-41,43,44 & PIN 8 ON ICs 3-5,9,10, 15,20,29,34,42.

+5V
C3 .047
C5 4.7µ
0V

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

FLB — INTEGRATION TIME LATCH

FROM IC3 PIN 9 CIRCUIT 31
FROM IC25 PIN 6 CIRCUIT 31
FROM IC25 PIN 8 CIRCUIT 31
FROM IC4 PIN 9 CIRCUIT 31
FROM IC20 PIN 6 CIRCUIT 31

IC28e 7404 (5→6)
IC34 CK a 7475 (D_1, $\bar{Q}_1$)
IC34 CK b 7475 (D_2, $\bar{Q}_2$)
R4 680 (+5V)
IC2f 7404 (13→12)
IC35d 7401 (11,12→13)
IC35c 7401 (9,8→10)

OUTPUT 1 → TO EC 42 B CIRCUIT 37 → 3A INTEGRATION TIME 1 (247)
OUTPUT 2 → TO EC 41 B CIRCUIT 37 → 2A INTEGRATION TIME 2 (248)

FLC — MEASURE DELAY LATCH

FROM IC3 PIN 10 CIRCUIT 31
FROM IC25 PIN 6 CIRCUIT 31
FROM IC25 PIN 8 CIRCUIT 31
FROM IC4 PIN 10 CIRCUIT 31
FROM IC26 PIN 8 CIRCUIT 31
FROM IC15 PIN 9 CIRCUIT 31

IC28c 7404 (9→8)
IC34 CK c 7475 (D_3, $\bar{Q}_3$)
IC34 CK d 7475 (D_4, $\bar{Q}_4$)
R29 680 (+5V)
IC28b 7404 (3→4)
IC27b 7401 (5,6→4)
R26 680 (+5V)
IC26a 7404 (1→2)
IC35b 7401 (5,6→4)
IC35a 7401 (3,2→1)

OUTPUT 1 → TO EC 42 B CIRCUIT 37 → 5A MEASURE DELAY 1 (324)
OUTPUT 2 → TO EC 41 B CIRCUIT 37 → 4A MEASURE DELAY 2 (325)
TO IC6 PIN 1 CIRCUIT 34

FLD — DISPLAY LATCH

FROM IC3 PIN 11 CIRCUIT 31
FROM IC25 PIN 6 CIRCUIT 31
FROM IC25 PIN 8 CIRCUIT 31
FROM IC4 PIN 11 CIRCUIT 31
FROM IC20 PIN 5 CIRCUIT 31

IC28d 7404 (11→10)
IC29 CK a 7475 (D_1, $\bar{Q}_1$)
IC29 CK b 7475 (D_2, $\bar{Q}_2$)
R5 680 (+5V)
IC2d 7404 (11→10)
IC30d 7401 (11,12→13)
IC30c 7401 (9,8→10)

OUTPUT 1 → TO EC 42 B CIRCUIT 37 → 20A DISPLAY CARTES (128)
OUTPUT 2 → TO EC 41 B CIRCUIT 37 → 19A DISPLAY LOG (127)

FLE — MEASUREMENT MODE LATCH

FROM IC3 PIN 12 CIRCUIT 31
FROM IC25 PIN 6 CIRCUIT 31
FROM IC25 PIN 8 CIRCUIT 31
FROM IC4 PIN 12 CIRCUIT 31
FROM IC26 PIN 8 CIRCUIT 31
FROM IC15 PIN 10 CIRCUIT 31

IC28f 7404 (13→12)
IC29 CK c 7475 (D_3, $\bar{Q}_3$)
IC29 CK d 7475 (D_4, $\bar{Q}_4$)
R28 680 (+5V)
IC28a 7404 (1→2)
IC27a 7401 (3,2→1)
R25 680 (+5V)
IC26b 7404 (3→4)
IC30b 7401 (5,6→4)
IC30a 7401 (3,2→1)

OUTPUT 1 → TO EC 42 B CIRCUIT 37 → 24A MEASURE X (347)
OUTPUT 2 → TO EC 41 B CIRCUIT 37 → 23A MEASURE Y (348)
TO IC6 PIN 5 CIRCUIT 34

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 33

SOURCE	SIG No.	DESTINATION
62	486	
62	438	29.73
	476	50.75
	415	64
	487	64
	122	73
	483	64
	484	64
	506	64 70
	313	36.73

PART OF BOARD 14 OF 1170
(A1709014)

FLF — MEASUREMENT LATCH

NOTE –
FOR POWER RAILS
SEE CIRCUIT 32

FROM IC3 PIN 7 CIRCUIT 31
FROM IC25 PIN 6 CIRCUIT 31
FROM IC25 PIN 8 CIRCUIT 31
FROM IC4 PIN 7 CIRCUIT 31
FROM IC20 PIN 4 CIRCUIT 31
RUN (438) 26A

FROM IC25 PIN 8 CIRCUIT 31
FROM IC6 PIN 9 CIRCUIT 31
FROM IC15 PIN 12 CIRCUIT 31
FROM IC9 PIN 12 CIRCUIT 31

+5V
R37 680
R1 680
R2 680
R3 680
7404
7400
7401
7474
IC37 b
IC37 c
IC37 d
IC16 c
IC39b
IC40 c
IC40 d
IC40 e
IC40 f
IC40 a
IC20 a
IC20 b
IC20 c
IC20 d
IC20 e
IC20 f

OUTPUT 1
OUTPUT 2

11A STOP (476)
7A RECYCLE (415)
6A SINGLE (487)
7B DISABLE DISPLAY (122)

IC3 PIN 7 CIRCUIT 35
IC3 PIN 12 CIRCUIT 34

FLG — SWEEP COMMAND LATCH

FROM IC3 PIN 4 CIRCUIT 31
SET SWEEP OFF (486) 10A
FROM IC7 PIN 12 CIRCUIT 31
FROM IC7 PIN 6 CIRCUIT 31
FROM IC4 PIN 4 CIRCUIT 31
FROM IC15 PIN 5 CIRCUIT 31

OUTPUT
OUTPUT 2
TO EC 42 B
TO EC 43 B

9A SWEEP CMD 1 (483)
8A SWEEP CMD 2 (484)

FLH — SWEEP MODE LATCH

FROM IC5 PIN 9 CIRCUIT 31
FROM IC10 PIN 12 CIRCUIT 31
FROM IC9 PIN 9 CIRCUIT 31
FROM IC15 PIN 4 CIRCUIT 31

OUTPUT 4
TO EC 40 B CIRCUIT 37

21B SWEEP MODE (506)
52B LOG/LIN TOUCH KEY PULSE (313)

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 34

SOURCE	SIG No.	DESTINATION
4	321	30.50.58.66
	163	
	593	
	237	
	125	20.52
74	251	75
	337	11.41
	16	12.41
	416	64

PART OF BOARD 14 OF 1170
(A1709014)

NOTE:—
FOR POWER RAILS
SEE CIRCUIT 32

FLJ

FROM IC5 PIN 7 CIRCUIT 31
FROM IC24 PIN 8 CIRCUIT 35
FROM IC25 PIN 8 CIRCUIT 31
FROM IC7 PIN 6 CIRCUIT 31
FROM IC26 PIN 2 CIRCUIT 32
FROM IC9 PIN 7 CIRCUIT 31
FROM IC25 PIN 6 CIRCUIT 31
FROM IC7 PIN 12 CIRCUIT 31
FROM IC7 PIN 10 CIRCUIT 31
FROM IC26 PIN 4 CIRCUIT 32
FROM IC25 PIN 6 CIRCUIT 31
FROM IC7 PIN 12 CIRCUIT 31
FROM IC7 PIN 10 CIRCUIT 31
FROM IC38 PIN 10 CIRCUIT 33
FROM IC9 PIN 6 CIRCUIT 31
FROM IC5 PIN 6 CIRCUIT 31
FROM IC25 PIN 8 CIRCUIT 31
FROM IC7 PIN 6 CIRCUIT 31
FROM IC2 PIN 8 CIRCUIT 35

INHIBIT DEMOD (237) 34B
1184 FITTED (595) 21A
FORCE MOD (163) 12A
MAINS SET (321) 1A

IC7b 7404
IC23a 7406
IC12b 7401
IC17c 846
IC6a 7400
IC7a 7404
IC23b 7406
IC12a 7401
IC17b 846
IC6b 7400
IC33 7401
IC23e 7406
IC18b 7401
IC7a 846
IC21d 7400
IC26c 7404
IC23c 7406
IC18a 7401
IC17d 846
IC21c 7400
IC23f 7406

+5V R16 680
+5V R9 680
+5V R12 2.2k
+5V R17 680
+5V R10 480
+5V R14 680
+5V R13 1k
+5V R15 680

IC 11a 7474
IC 11b 7474
IC 22b 7474
IC 22a 7474

IC16a 862
IC16b 862
IC1a 846
IC1b 846
IC18d 7401
IC18c 7401

CARRIER MODE LATCH

IC12c 7401 — 10 OUTPUT 2 → TO EC 41B CIRCUIT 37
IC12d 7401 — 13 OUTPUT 1 → TO EC 42B CIRCUIT 37

32A DEMOD (125)
26B INVALID (251)
32B MOD (337)

PART OF BOARD 25 (A1709025) MOTHERBOARD
SKJ
D13 → TO TOUCH KEY CARRIER LATCH SEE CIRCUIT 41
B13 → TO MODULATE SEE CIRCUIT 11
B12 → TO ADD BIAS SEE CIRCUIT 12
D12 → TO TOUCH KEY CARRIER LATCH SEE CIRCUIT 41

FLK

OUTPUT BIAS LATCH

OUTPUT 1 → TO EC 42 B CIRCUIT 37
OUTPUT 2 → TO EC 41B CIRCUIT 37

14A ADD BIAS (116)
15A REJECT BIAS (416)

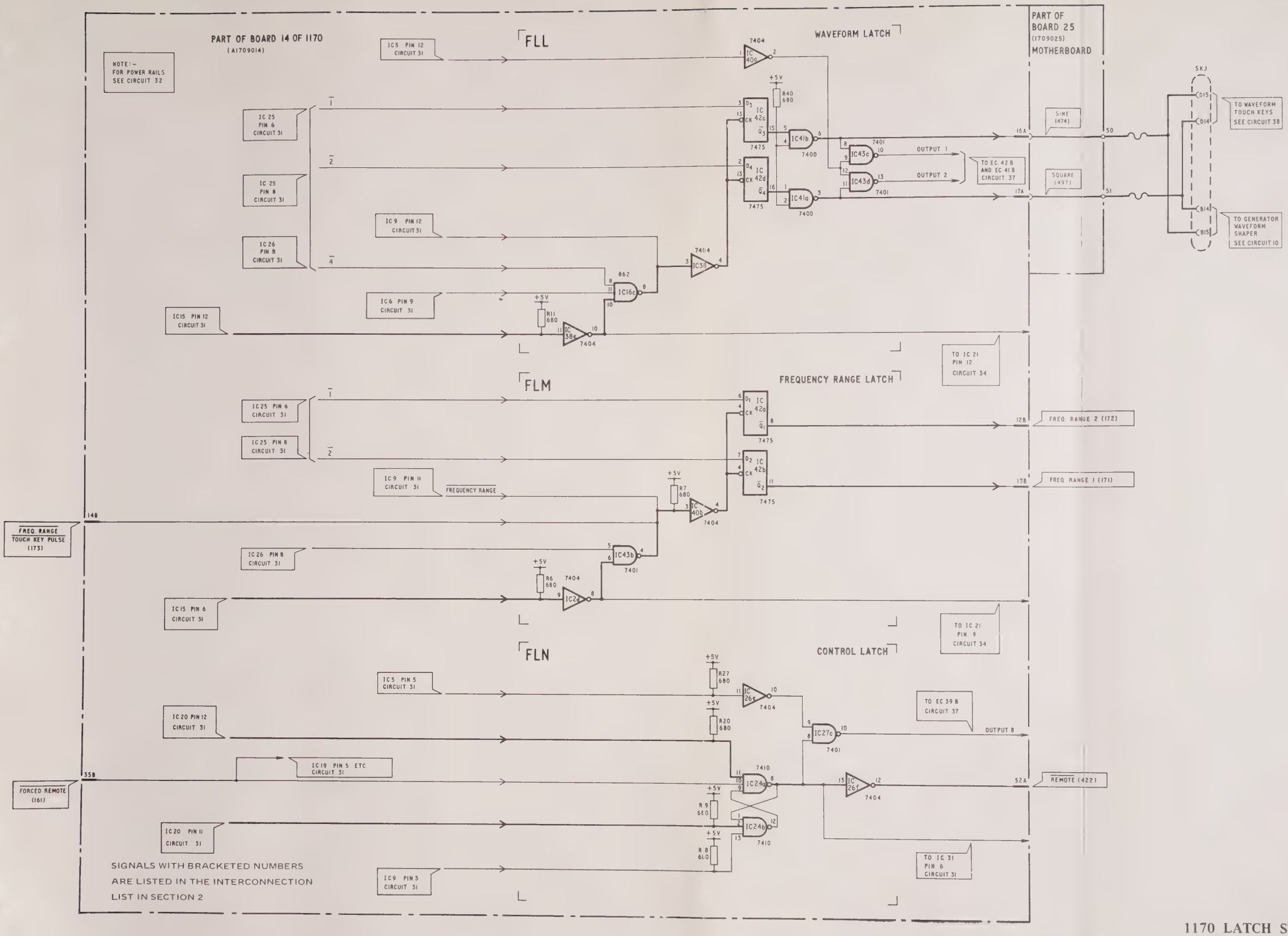
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 35

SOURCE	SIG No.	DESTINATION
	161	31
	173	71
	474	14.38
	497	10.38
	172	71
	171	71
	422	

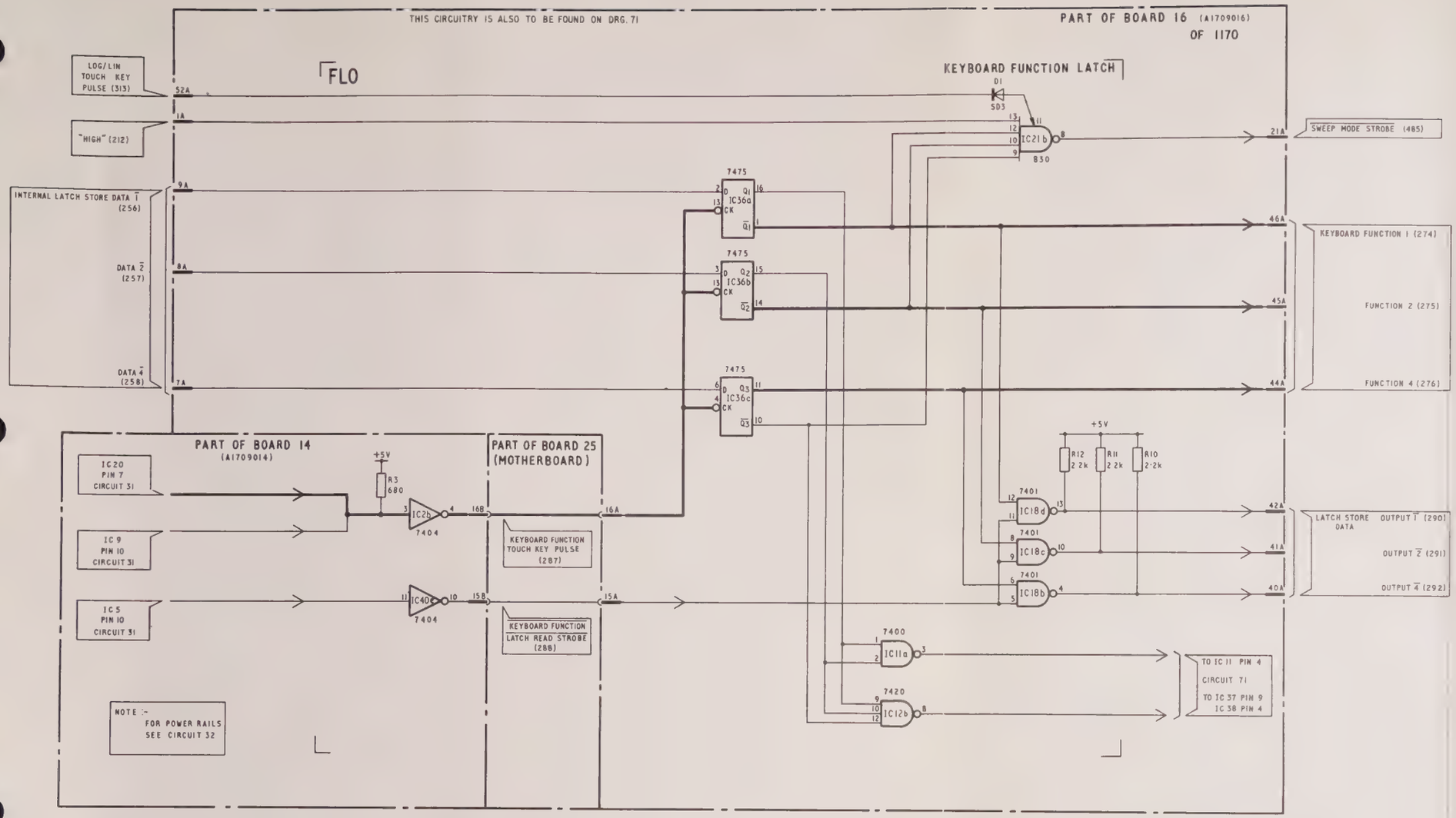

PART OF BOARD 14 OF 1170
(A1709014)
NOTE:- FOR POWER RAILS SEE CIRCUIT 32
FLL
WAVEFORM LATCH
PART OF BOARD 25
(1709025)
MOTHERBOARD
IC5 PIN 12 CIRCUIT 31
IC 25 PIN 6 CIRCUIT 31
IC 25 PIN 8 CIRCUIT 31
IC 26 PIN 8 CIRCUIT 31
IC9 PIN 12 CIRCUIT 31
IC6 PIN 9 CIRCUIT 31
IC15 PIN 12 CIRCUIT 31
7404
IC 40a
IC 42c
IC 42d
7475
R40 680
IC41b
IC41a
7400
7401
IC43c
IC43d
OUTPUT 1
OUTPUT 2
TO EC 42 B AND EC 41 B CIRCUIT 37
SINE (474)
SQUARE (497)
16A
17A
50
51
SKJ
D15
D14
B14
B15
TO WAVEFORM TOUCH KEYS SEE CIRCUIT 38
TO GENERATOR WAVEFORM SHAPER SEE CIRCUIT 10
862
IC16c
IC38
R11 680
IC38c
TO IC 21 PIN 12 CIRCUIT 34
FLM
FREQUENCY RANGE LATCH
IC 42a
IC 42b
IC 40b
R7 680
12B
FREQ. RANGE 2 (172)
13B
FREQ. RANGE 1 (171)
FREQUENCY RANGE
14B
FREQ. RANGE TOUCH KEY PULSE (173)
IC43b
R6 680
IC24
IC15 PIN 6 CIRCUIT 31
TO IC 21 PIN 9 CIRCUIT 34
FLN
CONTROL LATCH
IC 26e
IC 26f
R27 680
R20 680
IC27c
TO EC 39 B CIRCUIT 37
OUTPUT 8
IC19 PIN 5 ETC CIRCUIT 31
35B
FORCED REMOTE (161)
IC24a
IC24b
7410
R9 680
R8 680
52A
REMOTE (422)
IC20 PIN 11 CIRCUIT 31
IC20 PIN 12 CIRCUIT 31
IC9 PIN 5 CIRCUIT 31
TO IC 31 PIN 6 CIRCUIT 31
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 36

SOURCE	SIG No.	DESTINATION
31	258	70.71.73
31	257	70.71.73
31	256	70.71.73
31	212	70.71
33	313	71
71	485	70
71	274	70
71	275	70
71	276	70
71.73	290	37
71.73	291	37
71.73	292	37
	287	71
	288	71



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 37 See page 1.3.22

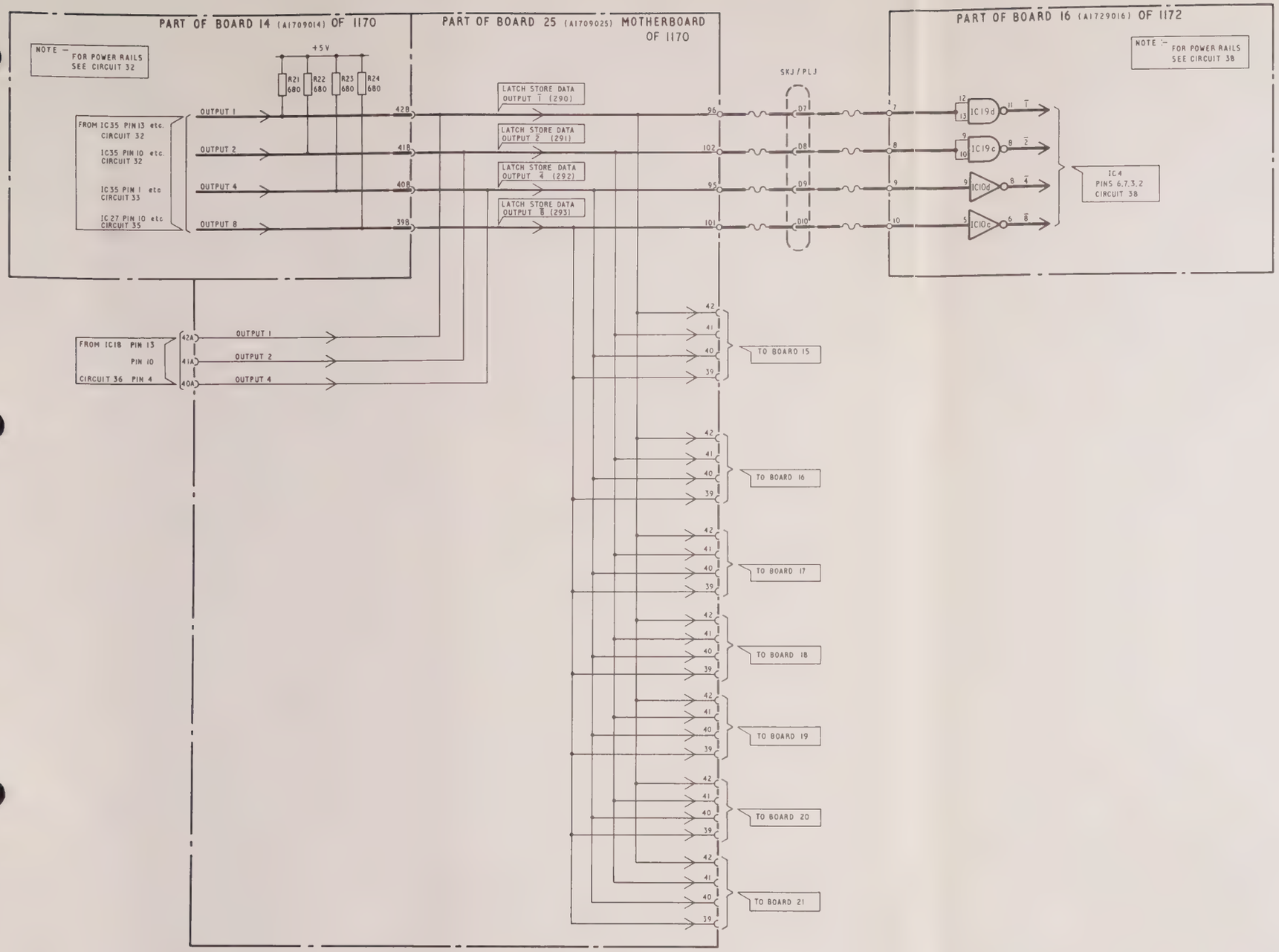
The Latch store outputs are connected together in this circuit to form the Latch Store Output Busses. The data held on these busses represents the contents of each store, in turn, in a 16 bit sequence at 500kHz.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 37

SOURCE	SIG No.	DESTINATION
36.71.73	290	37
36.71.73	291	37
36.71.73	292	37
73	293	37



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

LATCH STORE OUTPUT 37

D11707037-02

Circuit 38 See page 1.3.22

CIRCUITS 38 to 41

Each Touch Key Latch is strobed in turn from circuit No. 25. This causes the data held in the Latch Store to be copied into the latches on these circuits and the appropriate light to glow.

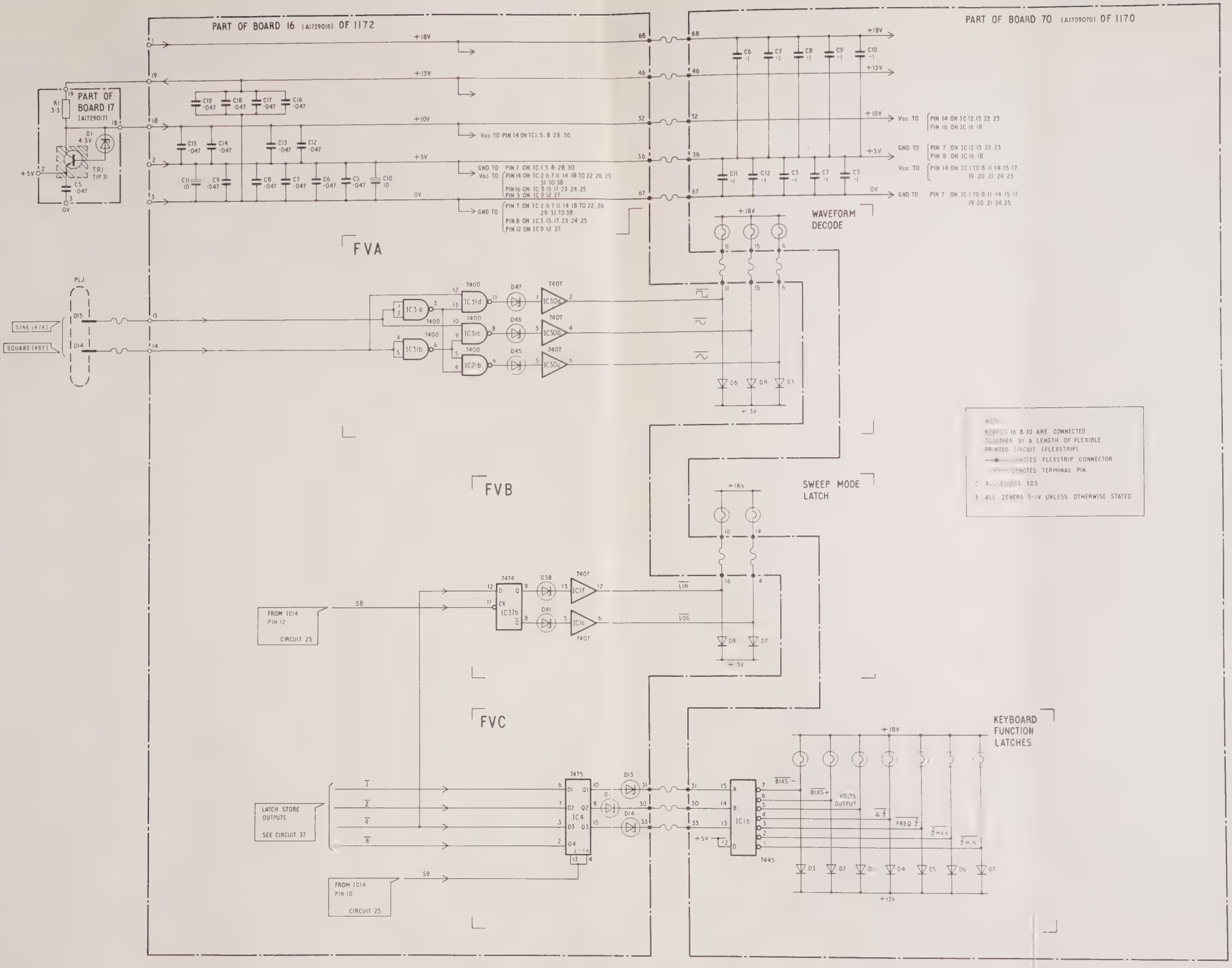
The Generator Mode, Modulate and Bias Add data are carried on single lines from the Latch Store and not strobed as are the others. This is because these data are used in other parts of the generator circuit.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 38

SOURCE	SIG No.	DESTINATION
35	497	10
35	474	14



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 39 See page 1.3.22

CIRCUITS 38 to 41

Each Touch Key Latch is strobed in turn from circuit No. 25. This causes the data held in the Latch Store to be copied into the latches on these circuits and the appropriate light to glow.

NOTE :-
1 FOR POWER RAILS SEE CIRCUIT 38
2 —●— DENOTES FLEXSTRIP CONNECTOR (SEE NOTE ON CIRCUIT 34)
3 ALL DIODES 5D3
4 ALL ZENERS ARE 5·1V

PART OF BOARD 16 (A1729016) OF 1172

FVD

FROM IC19 PIN 11 / CIRCUIT 37 / FROM IC19 PIN 8 — $\overline{1}$, $\overline{2}$

FROM IC26 PIN 12 / CIRCUIT 25 / FROM IC26 PIN 2 — S3, S4

7475 (IC27)

7400 IC18c, IC19a, IC18d, IC18b, IC18a, IC19b

7407 IC8e, IC8b, IC8d, IC8a, IC8f, IC8c

D55, D58, D54, D57, D56, D59

D18 D23 D26 D22 D15 D24 — +13V

PART OF BOARD 70 (A1709070) OF 1170

MODE & MEASUREMENT LATCHES

+18V

43 $\overline{X}$ · 49 $\overline{Y}$ · 53 $\overline{Y}$ · 48 SINGLE · 34 $\overline{STOP}$ · 50 $\overline{RECYCLE}$

D15 D16 D14 — +13V

D19 D17 D18 — +13V

FVE

DISPLAY & SWEEP COMMAND LATCHES

+18V

73 $\overline{a\ b}$ · 72 $\overline{R\ \theta}$ · 70 $\overline{LOG\ R\ \theta}$

D35 D34 D33 — +13V

FROM IC19 PIN 11 / CIRCUIT 37 / FROM IC19 PIN 8 — $\overline{1}$, $\overline{2}$

IC7 PIN 8 / CIRCUIT 25 / IC14 PIN 4 — S2, S7

7475 (IC12)

7400 IC21c, IC21d, IC21a, IC11b, IC11c, IC11a, IC11d

7407 IC30f, IC30e, IC30d, IC1e, IC1d, IC1a, IC1b

D44, D43, D42, D37, D36, D39, D40

$\overline{OFF}$ · $\overline{HOLD}$ · ↑ · ↓

+18V

5 1 9 10 — 5 1 9 10

D2 D1 D4 D5 — +13V

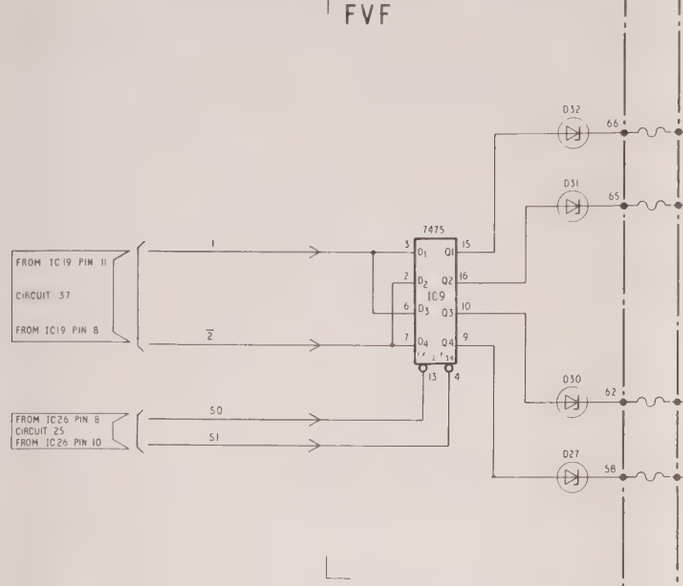
Circuit 40 See page 1.3.22

CIRCUITS 38 to 41

Each Touch Key Latch is strobed in turn from circuit No. 25. This causes the data held in the Latch Store to be copied into the latches on these circuits and the appropriate light to glow.

PART OF BOARD 16 (A1729016) OF PLUG-IN

FVF



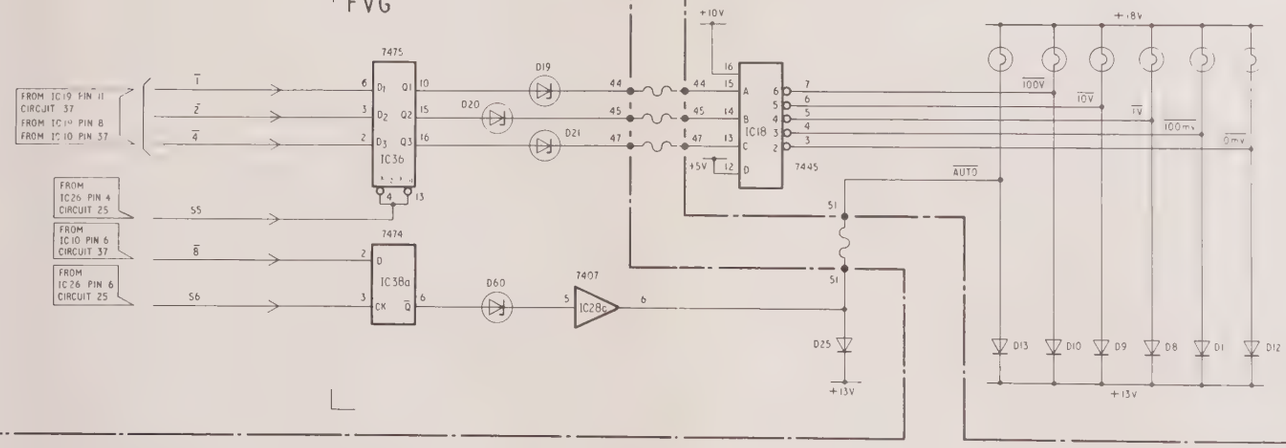
PART OF BOARD 70 (A1709070) OF 1170

INTEGRATION TIME & MEASUREMENT DELAY

NOTE –

1. FOR POWER RAILS SEE CIRCUIT 38
2. —●— DENOTES FLEX STRIP CONNECTOR
   —○— DENOTES TERMINAL PIN (SEE NOTE ON CIRCUIT 38)
3. ALL DIODES ARE SD3
4. ALL ZENERS ARE 5·1V

FVG



INPUT RANGE & AUTO RANGE LATCHES

CIRCUITS 38 to 41

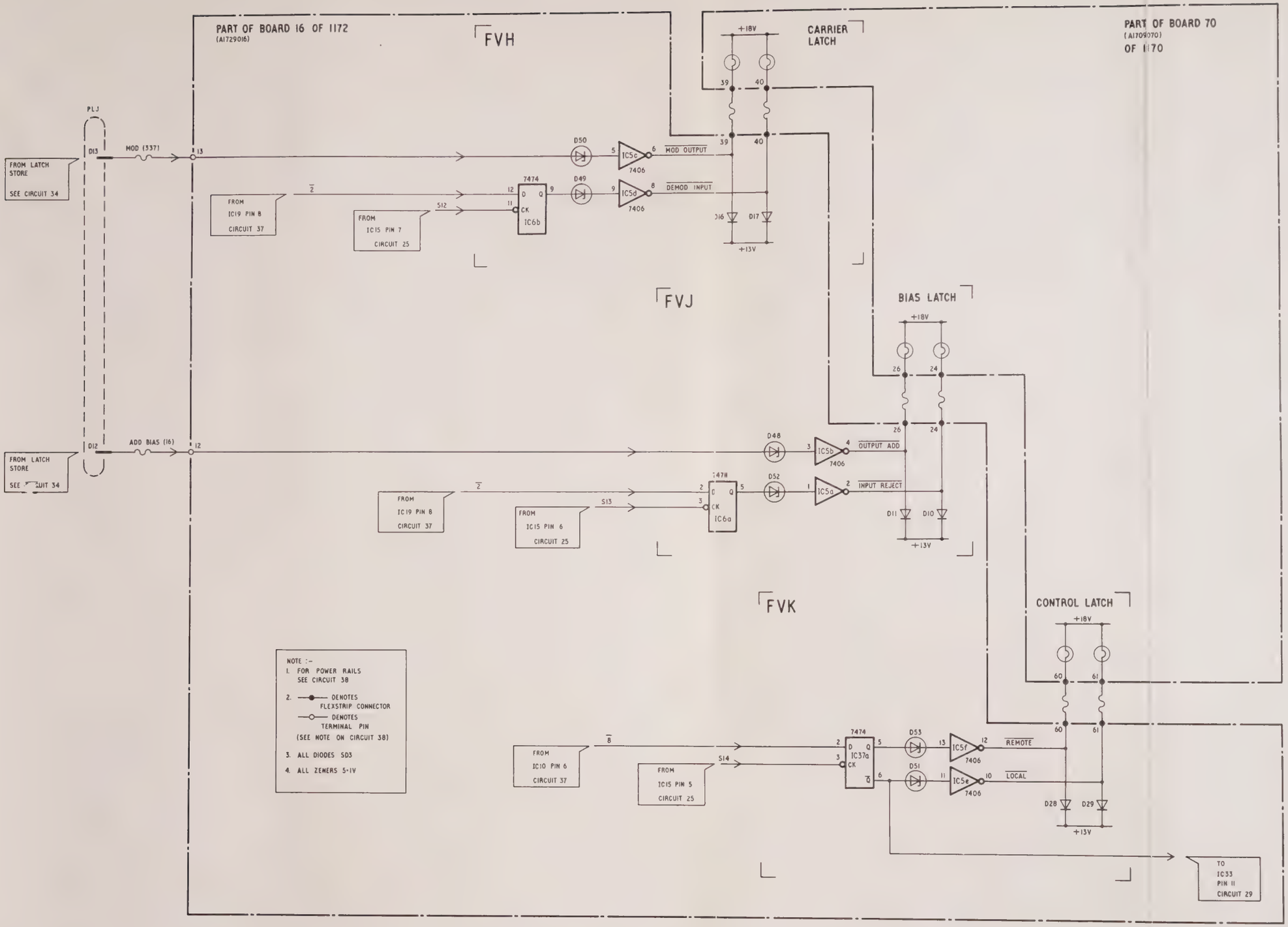
Each Touch Key Latch is strobed in turn from circuit No. 25. This causes the data held in the Latch Store to be copied into the latches on these circuits and the appropriate light to glow.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 41

SOURCE	SIG No.	DESTINATION
34	16	12
34	337	11

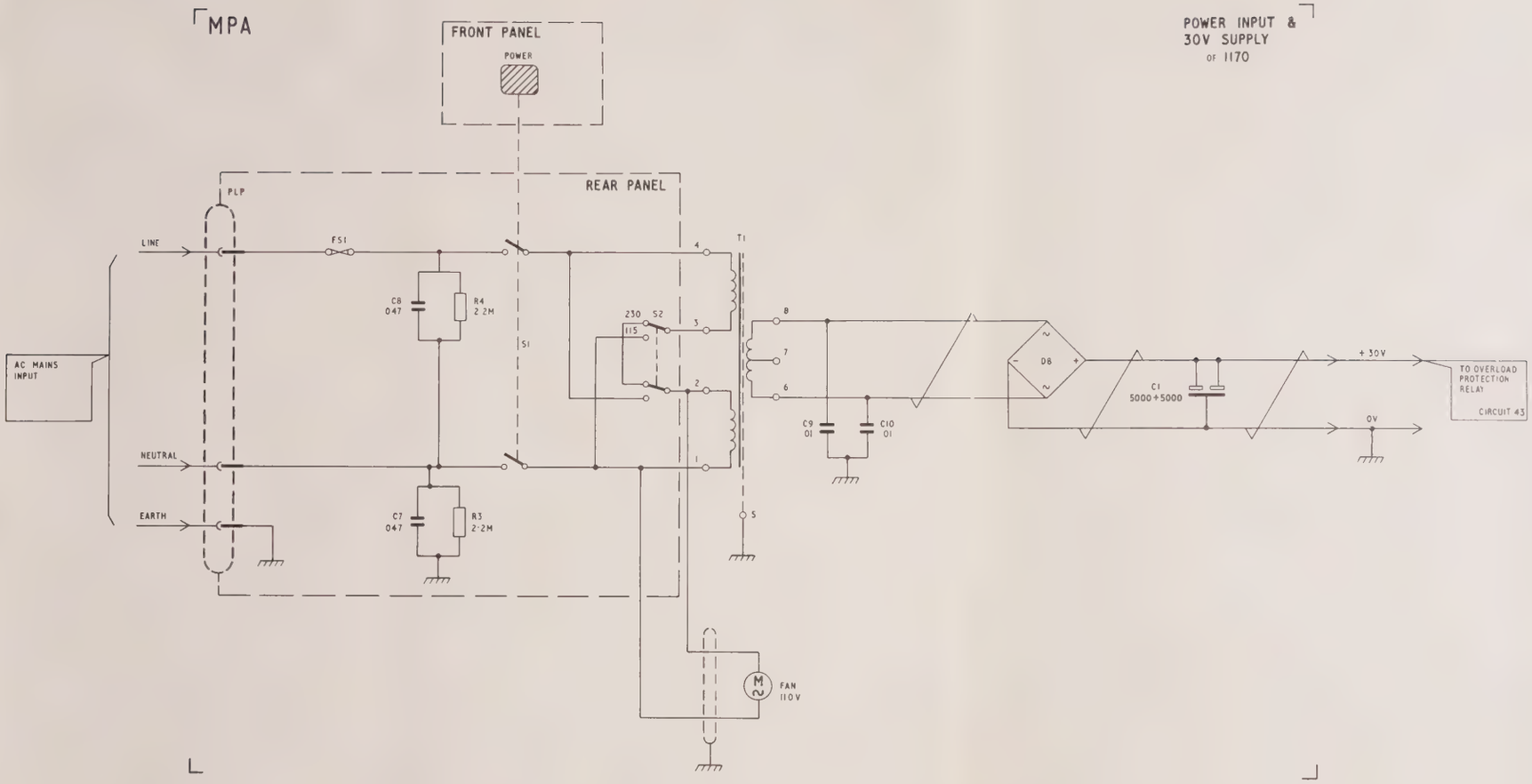


SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 42 See page 1.3.8

MPA

POWER INPUT &
30V SUPPLY
OF 1170



Circuit 43 See page 1.3.8

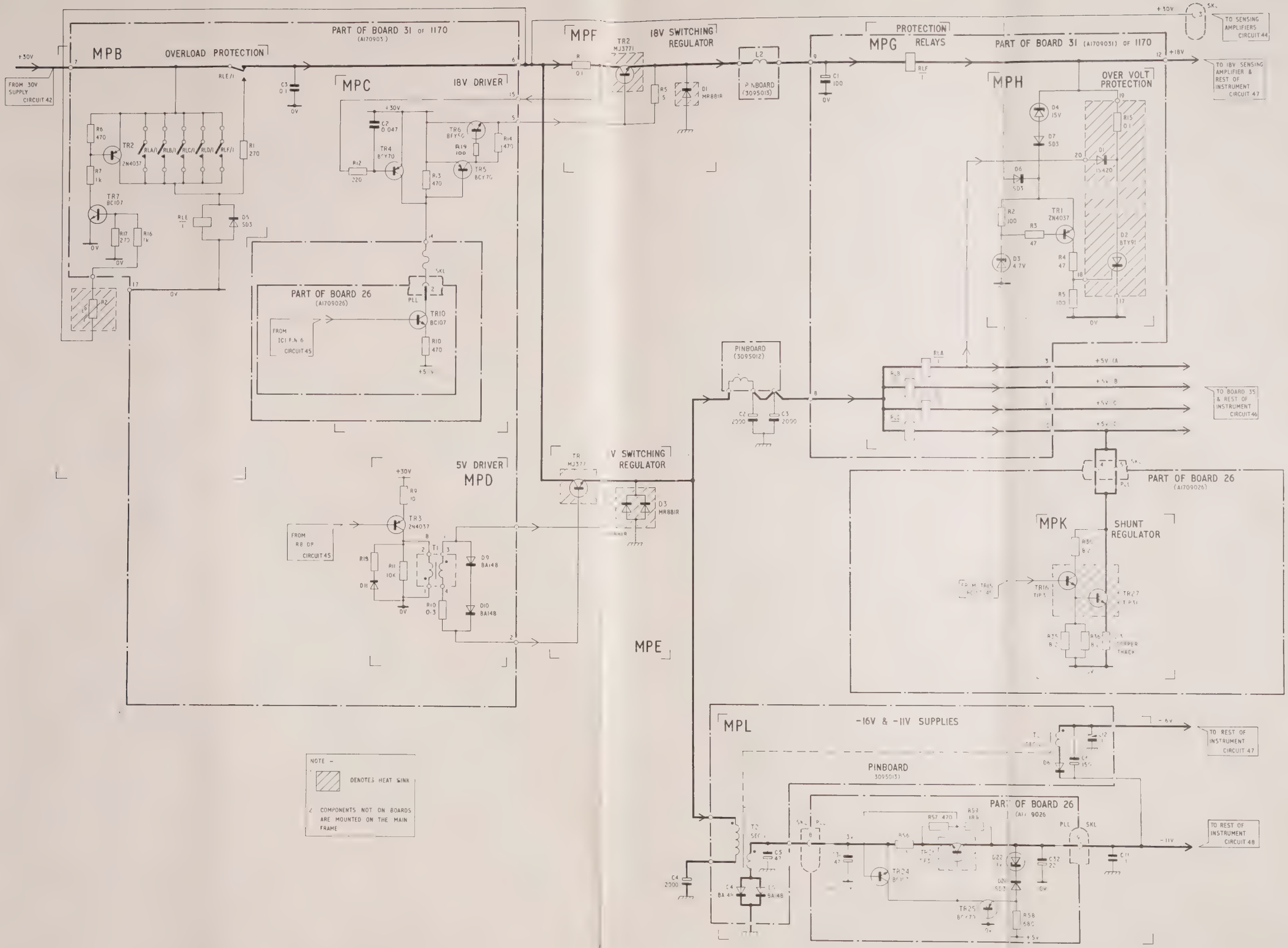
POWER SUPPLIES

Power is derived from the +30V rail. This voltage is dropped to +18V and +5V by the switching regulators. The regulating elements TR1 and TR2 (MJ3771) are switched at 25kHz, the mark to space ratio deciding the regulated voltage.

The +5V supply is split into four separate rails, one of them (D) having its own shunt regulator. The D rail supplies the plug in peripheral positions and therefore has a variable load.

The unsmoothed +5V supply, which has a large 25kHz component, is used to supply the primary of the +11V and +16V supply transformer.

Each of the major rails has a series relay coil, the contacts of which are used to trip the +30V rail in the event of an overload ($> 6A$). In addition the +5V (D) rail will be overloaded, and so cause a trip, if an excess voltage is detected on the +18V rail.


MPB
OVERLOAD PROTECTION
PART OF BOARD 31 OF 1170
(AI709031)
FROM 30V SUPPLY CIRCUIT 42
+30V
RLE/I
C3 0.1
0V
MPC
18V DRIVER
R6 470
TR2 2N4037
RLA/I
RLB/I
RLC/I
RLD/I
RLF/I
R1 270
R7 1k
TR7 BC107
R17 270
R16 1k
RLE I
D5 S03
R2
C2 0.047
TR4 BCY70
R12 220
R3 470
TR6 BFY50
R19 100
TR5 BCY70
R14 1470
PART OF BOARD 26
(AI709026)
FROM IC1 P.N 6 CIRCUIT 45
SKL
PLL
TR10 BC107
R10 470
+5 V
MPF
18V SWITCHING REGULATOR
R 0.1
TR2 MJ3771
R5 5
D1 MR881R
L2
P NBOARD (3095013)
MPG
PROTECTION RELAYS
C1 100
RLF
MPH
OVER VOLT PROTECTION
D4 15V
D7 S03
D6 S03
R2 100
TR1 ZN4037
R3 47
D3 4.7V
R4 47
R5 10Ω
D1 1S420
D2 BTY91
R15 0.1
PINBOARD (3095012)
C2 2000
C3 2000
RLA
RLB
RLC
+5V (A
+5V B
+5V C
+5V
TO BOARD 35 & REST OF INSTRUMENT CIRCUIT 46
+30V
SK
TO SENSING AMPLIFIERS CIRCUIT 44
+18V
TO 18V SENSING AMPLIFIER & REST OF INSTRUMENT CIRCUIT 47
PART OF BOARD 26
(AI709026)
MPK
SHUNT REGULATOR
TR16 TIP3
TR17 TIP31
MPD
5V DRIVER
+30V
R9 10
TR3 2N4037
FROM R8 DP CIRCUIT 45
R18
R11 10K
D11
T1
D9 BA148
D10 BA148
R10 0.3
0V
TR MJ3771
D3 MR881R
V SWITCHING REGULATOR
MPE
MPL
-16V & -11V SUPPLIES
PINBOARD 3095013
PART OF BOARD 26
(AI709026)
T2 SEC
C5 47
C4 2000
D4 BA148
D5 BA148
TR24 BC477
TR25 BC477
R57 470
R56
R58 680
D22 1V
C32 22
C11 1
-6V
-11V
TO REST OF INSTRUMENT CIRCUIT 47
TO REST OF INSTRUMENT CIRCUIT 48
NOTE –
DENOTES HEAT SINK
COMPONENTS NOT ON BOARDS ARE MOUNTED ON THE MAIN FRAME

Circuit 44 See page 1.3.8

This circuit provides the necessary floating supplies for the input circuits (pcb's 23 and 24) and the 1184 peripheral (position 22).

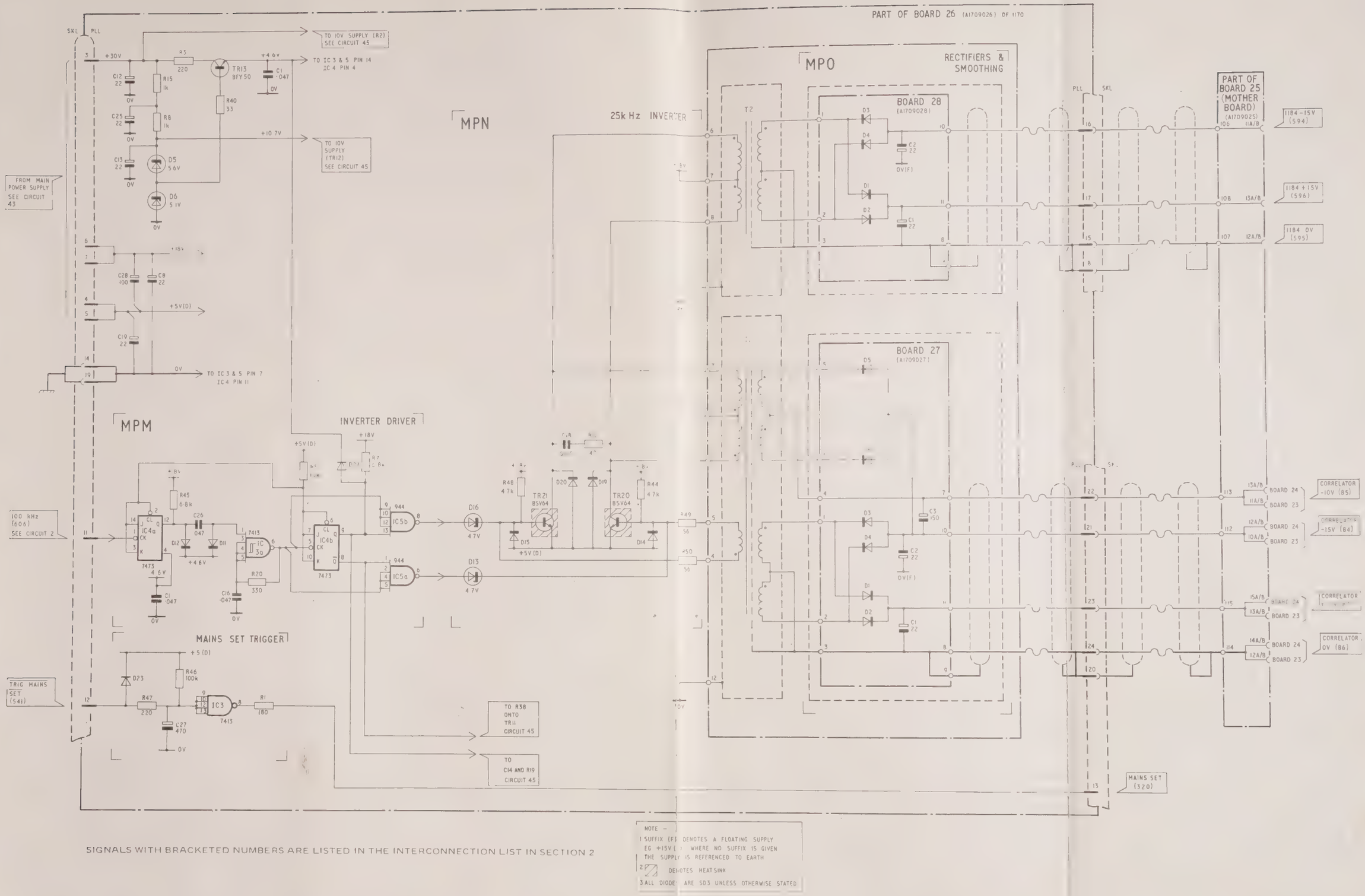
The 25kHz switching frequency used for the inverter and for the main switching regulators (circuits 45 and 43) is derived by dividing the 100kHz obtained from 1172/77 module.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 44

SOURCE	SIG No.	DESTINATION
68	541	
2	606	17.54
	594	
	596	
	595	
	85	
	84	
	87	
	86	
	320	4



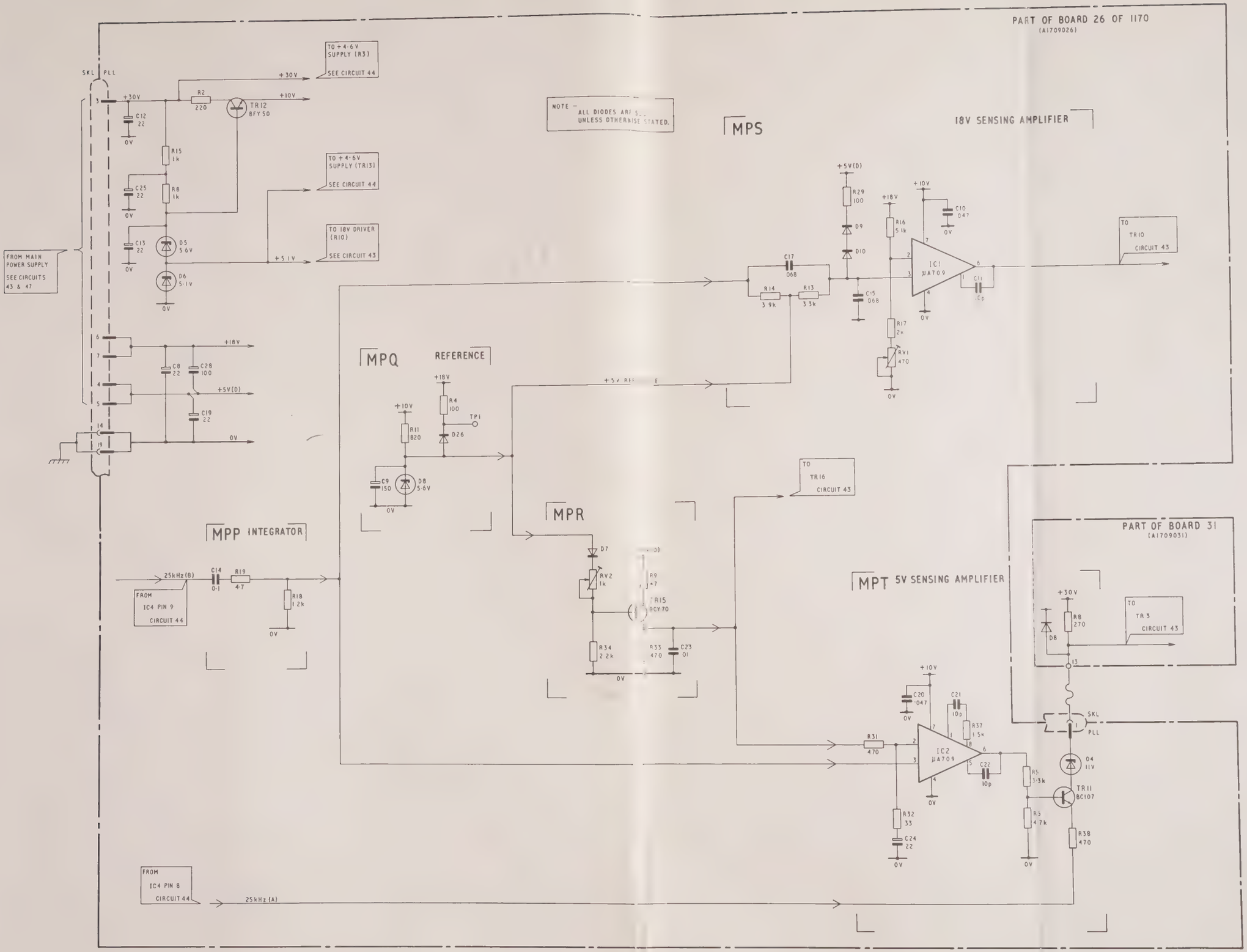
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

NOTE –
1 SUFFIX (F) DENOTES A FLOATING SUPPLY EG +15V (F) WHERE NO SUFFIX IS GIVEN THE SUPPLY IS REFERENCED TO EARTH
2 DENOTES HEATSINK
3 ALL DIODES ARE SD3 UNLESS OTHERWISE STATED

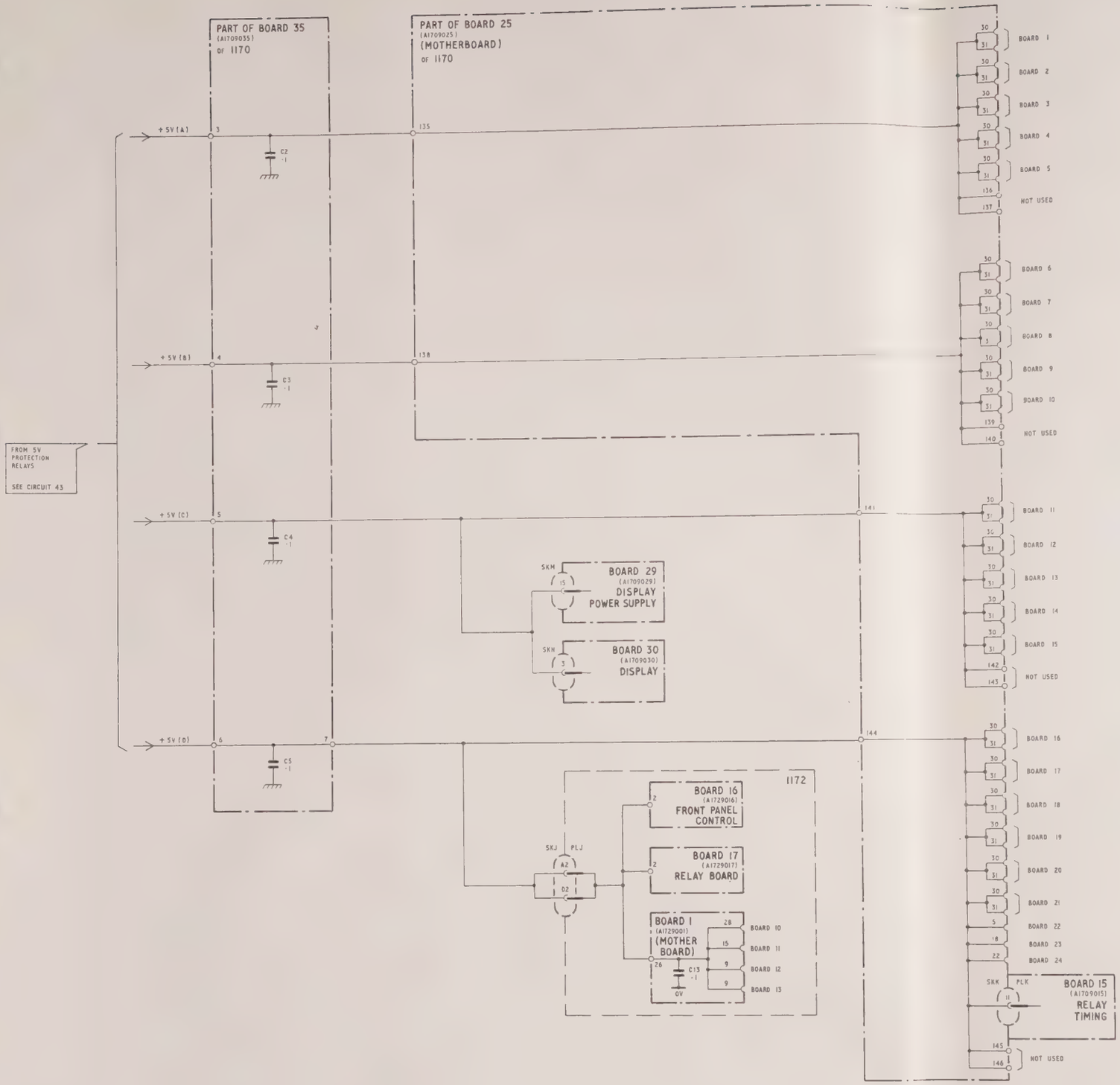
Circuit 45 See page 1.3.8

IC1 and IC2 have a 25kHz square wave input on terminal 3 and a variable dc input to terminal 2. The variable input is proportional to the sensed +18V or +5V rails. The outputs of ICs 1 and 2 are 25kHz square wave with mark to space ratios proportional to the +5V or +18V rails.

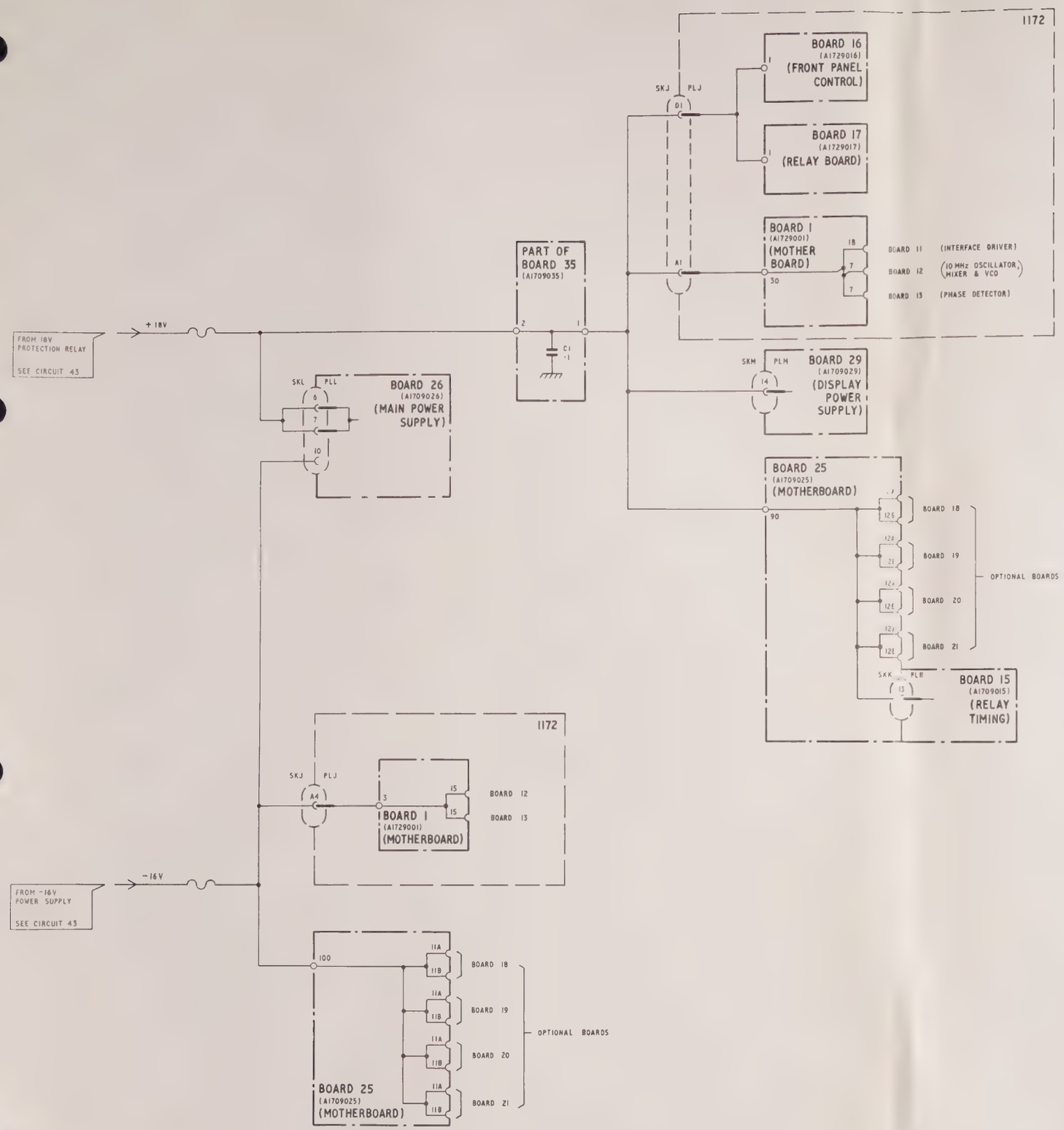
The output from block MPR to TR16 is a dc voltage proportional to the +5V (D) rail.


PART OF BOARD 26 OF 1170
(A1709026)
SKL PLL
FROM MAIN POWER SUPPLY
SEE CIRCUITS 43 & 47
+30V
+10V
+18V
+5V(D)
+5.1V
0V
R2 220
TR12 BFY50
C12 22
R15 1k
C25 22
R8 1k
C13 22
D5 5.6V
D6 5.1V
TO +4·6V SUPPLY (R3)
SEE CIRCUIT 44
TO +4·6V SUPPLY (TR13)
SEE CIRCUIT 44
TO 18V DRIVER (R10)
SEE CIRCUIT 43
C8 22
C28 100
C19 22
NOTE – ALL DIODES ARE S... UNLESS OTHERWISE STATED.
MPS
18V SENSING AMPLIFIER
R29 100
D9
D10
C17 068
R14 3·9k
R13 3·3k
C15 068
R16 5·1k
C10 047
IC1 µA709
C11 ·Cp
TO TR10 CIRCUIT 43
R17 2k
RV1 470
MPQ REFERENCE
R4 100
TP1
D26
R11 820
C9 150
D8 5·6V
MPR
D7
RV2 1k
R9 1·7
TR15 BCY70
R34 2·2k
R33 470
C23 01
TO TR16 CIRCUIT 43
MPP INTEGRATOR
25kHz(B)
FROM IC4 PIN 9 CIRCUIT 44
C14 0·1
R19 4·7
R18 1·2k
MPT 5V SENSING AMPLIFIER
PART OF BOARD 31
(A1709031)
+30V
R8 270
D8
TO TR3 CIRCUIT 43
C20 ·047
C21 10p
R37 1·5k
IC2 µA709
C22 10p
R31 470
R32 33
C24 22
R5 3·3k
R5 4·7k
SKL PLL
D4 11V
TR11 BC107
R38 470
FROM IC4 PIN 8 CIRCUIT 44
25kHz(A)

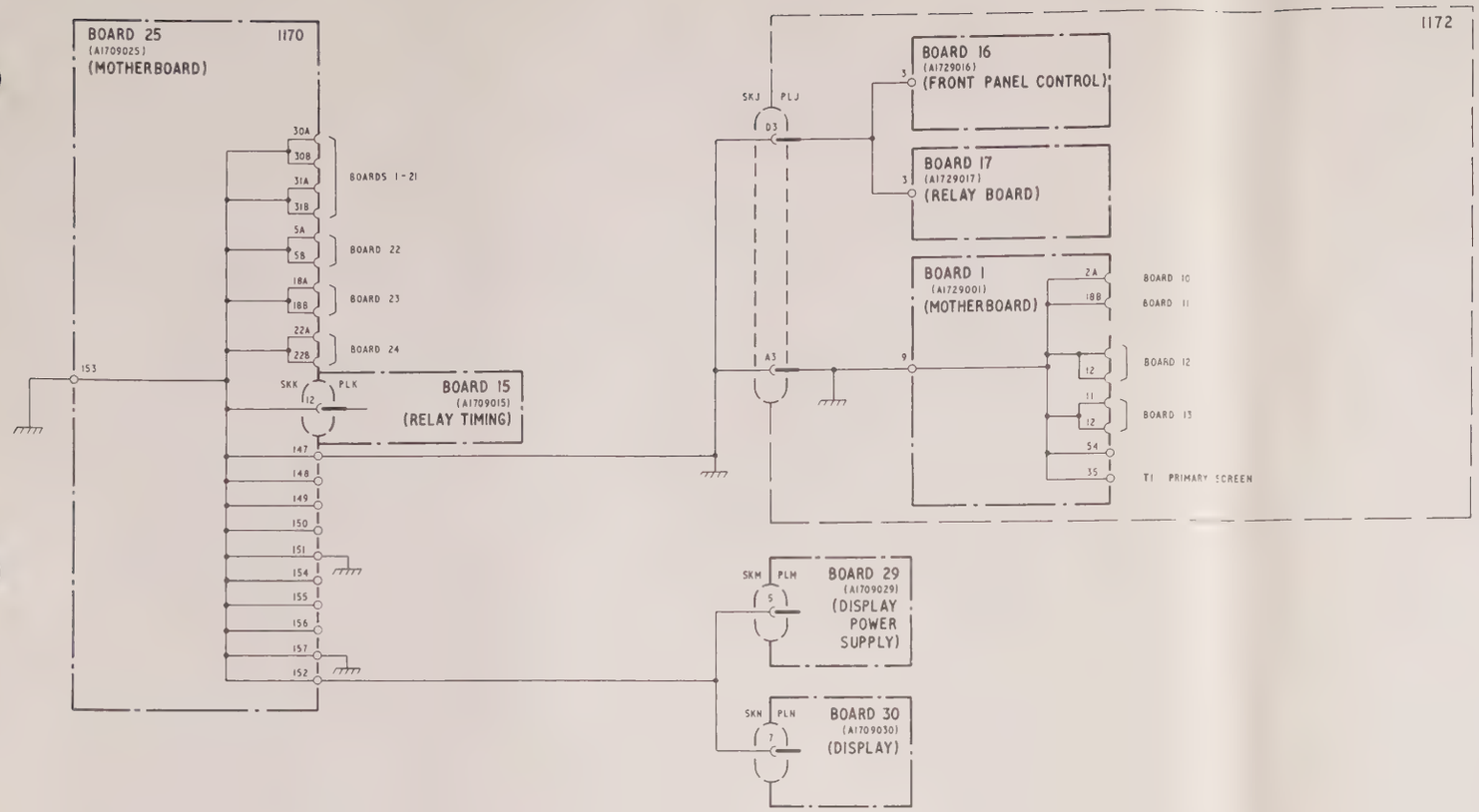
Circuit 46 See page 1.3.8

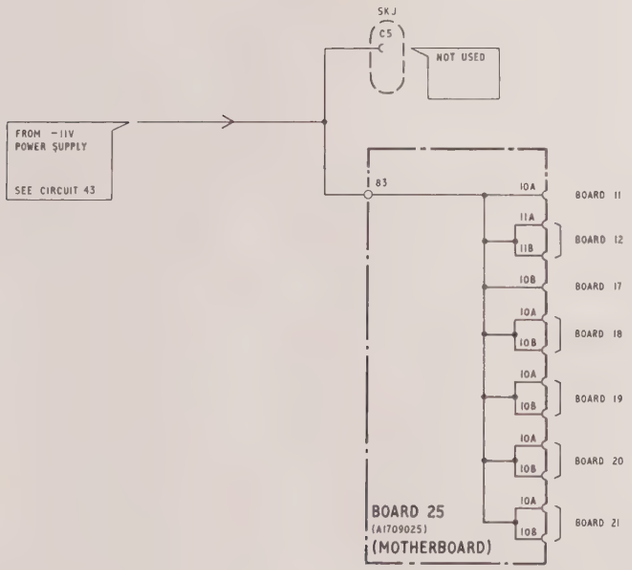

PART OF BOARD 35
(A1709035)
OF 1170
PART OF BOARD 25
(A1709025)
(MOTHERBOARD)
OF 1170
+5V (A)
+5V (B)
+5V (C)
+5V (D)
C2 ·1
C3 ·1
C4 ·1
C5 ·1
FROM 5V PROTECTION RELAYS
SEE CIRCUIT 43
135
138
141
144
BOARD 1
BOARD 2
BOARD 3
BOARD 4
BOARD 5
NOT USED
BOARD 6
BOARD 7
BOARD 8
BOARD 9
BOARD 10
NOT USED
BOARD 11
BOARD 12
BOARD 13
BOARD 14
BOARD 15
NOT USED
BOARD 16
BOARD 17
BOARD 18
BOARD 19
BOARD 20
BOARD 21
BOARD 22
BOARD 23
BOARD 24
BOARD 15
(A1709015)
RELAY TIMING
NOT USED
SKM
BOARD 29
(A1709029)
DISPLAY POWER SUPPLY
SKN
BOARD 30
(A1709030)
DISPLAY
1172
BOARD 16
(A1729016)
FRONT PANEL CONTROL
BOARD 17
(A1729017)
RELAY BOARD
SKJ
PLJ
BOARD 1
(A1729001)
(MOTHER BOARD)
C13 ·1
0V
BOARD 10
BOARD 11
BOARD 12
BOARD 13
SKK
PLK

Circuit 47 See page 1.3.8


1172
BOARD 16
(A1729016)
(FRONT PANEL CONTROL)
BOARD 17
(A1729017)
(RELAY BOARD)
BOARD 1
(A1729001)
(MOTHER BOARD)
BOARD 11 (INTERFACE DRIVER)
BOARD 12 (10 MHz OSCILLATOR, MIXER & VCO)
BOARD 13 (PHASE DETECTOR)
SKJ
PLJ
PART OF BOARD 35
(A1709035)
C1 .1
+18V
FROM 18V PROTECTION RELAY
SEE CIRCUIT 43
SKM
PLM
BOARD 29
(A1709029)
(DISPLAY POWER SUPPLY)
SKL
PLL
BOARD 26
(A1709026)
(MAIN POWER SUPPLY)
BOARD 25
(A1709025)
(MOTHERBOARD)
BOARD 18
BOARD 19
BOARD 20
BOARD 21
OPTIONAL BOARDS
SKK
PLK
BOARD 15
(A1709015)
(RELAY TIMING)
1172
BOARD 1
(A1729001)
(MOTHERBOARD)
BOARD 12
BOARD 13
-16V
FROM -16V POWER SUPPLY
SEE CIRCUIT 43
BOARD 25
(A1709025)
(MOTHERBOARD)
BOARD 18
BOARD 19
BOARD 20
BOARD 21
OPTIONAL BOARDS

Circuit 48 See page 1.3.8


BOARD 25
(A1709025)
(MOTHERBOARD)
1170
30A
30B
31A
31B
BOARDS 1-21
5A
5B
BOARD 22
18A
18B
BOARD 23
22A
22B
BOARD 24
153
SKK
PLK
12
BOARD 15
(A1709015)
(RELAY TIMING)
147
148
149
150
151
154
155
156
157
152
1172
SKJ
PLJ
D3
BOARD 16
(A1729016)
(FRONT PANEL CONTROL)
BOARD 17
(A1729017)
(RELAY BOARD)
BOARD 1
(A1729001)
(MOTHERBOARD)
A3
9
2A
BOARD 10
18B
BOARD 11
12
BOARD 12
11
12
BOARD 13
54
35
T1 PRIMARY SCREEN
SKM
PLM
5
BOARD 29
(A1709029)
(DISPLAY POWER SUPPLY)
SKN
PLN
7
BOARD 30
(A1709030)
(DISPLAY)


SKJ
C5
C
NOT USED
FROM -11V POWER SUPPLY
SEE CIRCUIT 43
83
10A
BOARD 11
11A
11B
BOARD 12
10B
BOARD 17
10A
10B
BOARD 18
10A
10B
BOARD 19
10A
10B
BOARD 20
10A
10B
BOARD 21
BOARD 25
(A1709025)
(MOTHERBOARD)

Circuit 50

This is one of the digital control circuits. A theoretical description is found in the description of the Arithmetic Unit (p. 1.3.39).

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. **50**

SOURCE	SIG No.	DESTINATION
73	10	64
32	248	
32	247	
32	324	
32	325	
33	476	75
56	97	
2	599	19.54
52	349	
52	645	
2	600	54
62	323	20.52.56
2	601	54
4	321	30.34.58.66
54	245	
	147	
	249	
69	169	
66	339	3.63.69.70.71.72.74
66	340	3.63.70.71.72.74.
66	341	3.63.70.71.72.73.74
66	342	3.63.70.71.72.74
2	611	21.25.54.58.65.66.69.70.72
2	607	
1	489	
8	388	
	149	
	614	
	613	
	605	8
	387	52
	250	
	463	8.52
	185	8.52
	210	20.52
	521	54
	144	54

BOARD 2 OF 1170
(A1709002)

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

N CYCLE COUNTER AND GENERATOR DIVIDER

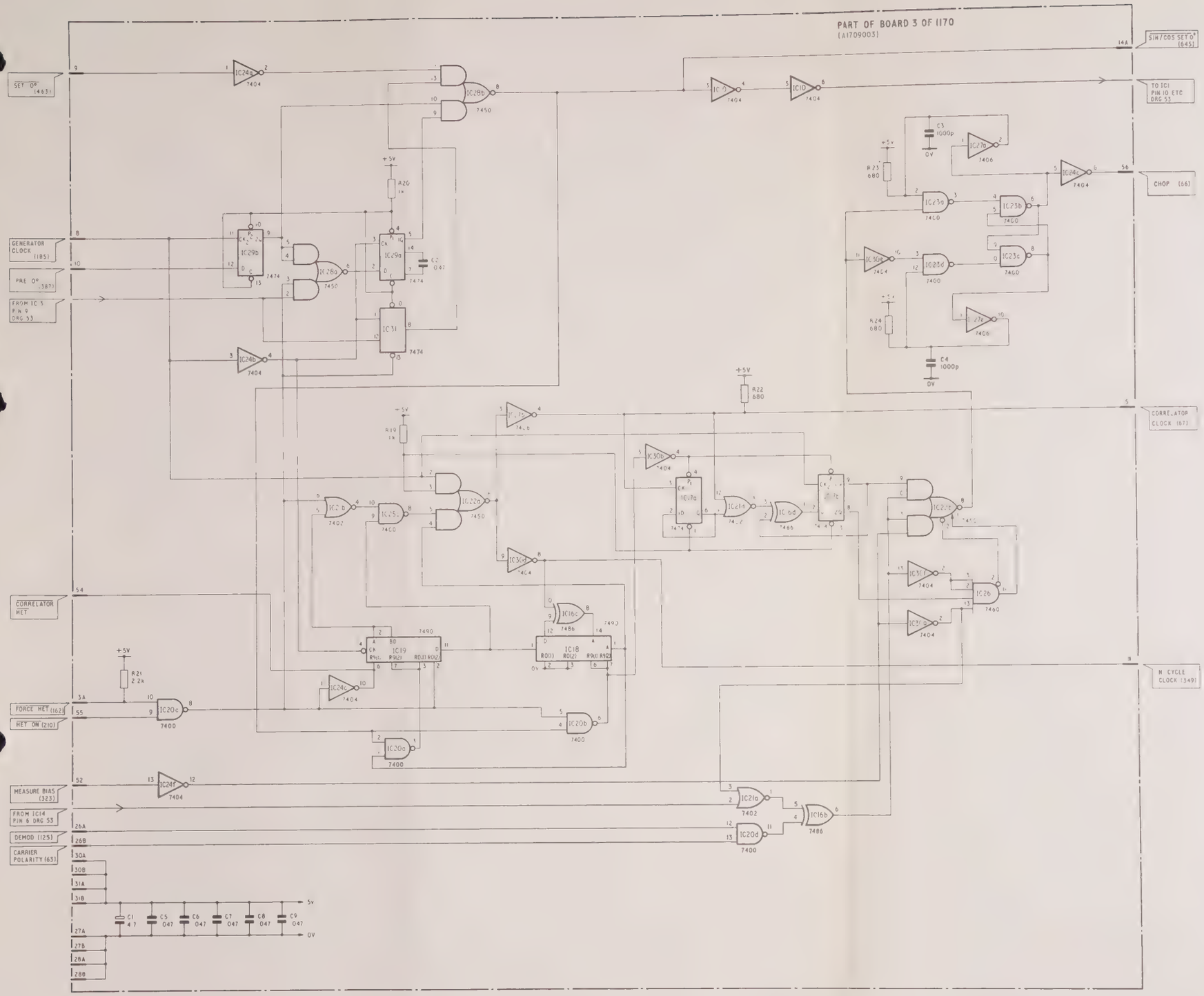
D11707050 - D

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 52

SOURCE	SIG No.	DESTINATION
	63	
34	125	20
62	323	20.50.56
50	210	20
	162	
50	387	
50	185	8
50	463	8
	645	50
	66	21
	67	53
	349	50



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 53

SOURCE	SIG No.	DESTINATION
	67	52
54	550	
	461	55
55	471	
55	470	
55	469	
55	468	
55	467	
55	466	
55	465	
55	464	
	460	55A
	79	55A
	78	55A
	77	55A
	76	55A
	75	55A
	74	55A
	73	55A
	72	55A

PART OF BOARD 3 OF 1170
(A1709003)

ROM TRUTH TABLE			
ADDRESS	OUTPUT	ADDRESS	OUTPUT
5	3	18	74
6	9	19	78
7	15	20	82
8	22	21	85
9	27	22	88
10	34	23	91
11	39	24	93
12	45	25	95
13	50	26	97
14	56	27	98
15	61	28	99
16	66	29	99
17	70	OTHERS	NOT USED

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

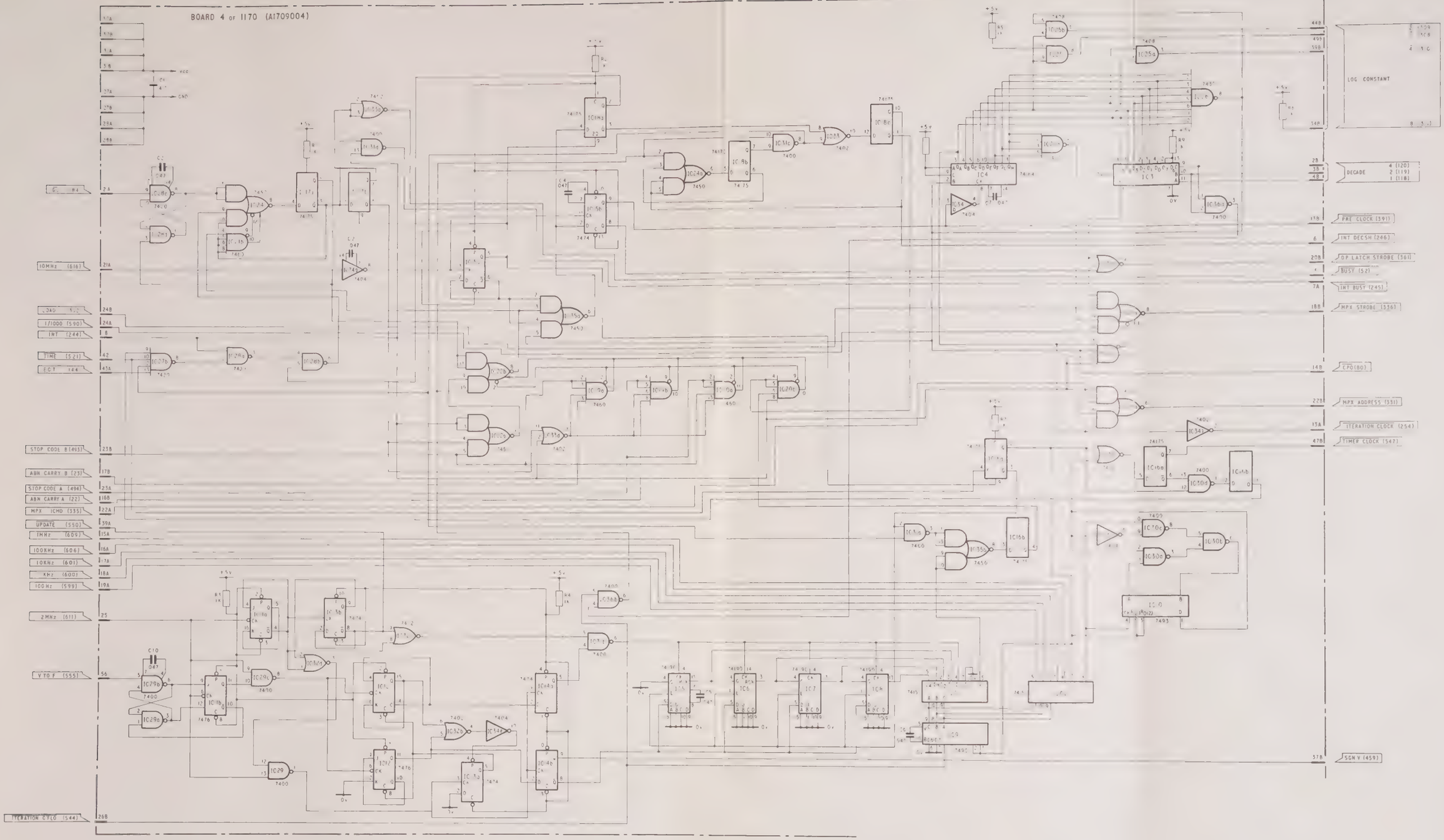
Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 54

SOURCE	SIG No.	DESTINATION
57	544	
21	555	
2	611	21.25.50.58.65.66.69.70.72
2	599	19.50
2	600	50
2	601	50
2	606	17.44
2	609	
	550	53
56	335	
55	22	
56	494	
55A	23	
56	493	
50	144	
50	521	
56	244	55.57
56	590	
56	302	55.55A
2	616	
64	184	
55	309	
55	308	
55	310	
55	311	
64	120	56.57
64	119	56.57
64	118	56.57
	391	55.55A
	246	56
	361	55.55A
	52	56.57.64
	245	50
	336	55.55A
	80	55.55A
	331	55.55A
	254	56.57
	547	57
	459	55.55A

BOARD 4 OF 1170 (A1709004)



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Alternative list for board 5
when fitted in position 6.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 55A

SOURCE	SIG No.	DESTINATION
54	336	55
56	334	
56	332	55
54	331	55
54	361	55
56	115	55
61	136	56
56	114	55
56	124	55
56	478	
56	302	54.55
54	80	55
56	234	55
55	385	56
54	391	55
56	11	55
56	12	55
56	64	55
56	244	54.55.57
53	460	
54	459	55
	117	56
	23	54
55	5	
55	9	
53	79	
55	38	
55	34	

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 55A (cont.)

SOURCE	SIG No.	DESTINATION
53	75	
55	4	
55	37	
55	8	
53	78	
55	33	
53	74	
	386	55.56
55	3	
55	36	
55	7	
53	77	
55	32	
53	73	
55	2	
55	35	
55	6	
53	76	
55	31	
53	72	
E	307	56.57.63.55
E	306	56.57.63.55
E	305	56.57.63.55
E	304	56.57.63.55

Circuit 55 See page 1.3.59

This pcb is duplicated and fitted in position 5 and 6 of the 1170.

In some cases the use made of the edge connectors differs between the two positions.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 55

SOURCE	SIG No.	DESTINATION
54	336	55A
56	333	
56	332	55A
54	331	55A
54	361	55A
56	115	55A
61	135	56
56	114	55A
56	124	55A
56	477	
56	302	54.55A
54	80	55A
56	234	55A
55A	386	56
54	391	55A
56	12	55A
56	11	55A
56	64	55A
56	244	54.57.55A
53	461	
54	459	55A
	116	56
	22	54
55A	34	
54	311	
55A	38	
53	471	
	9	55A

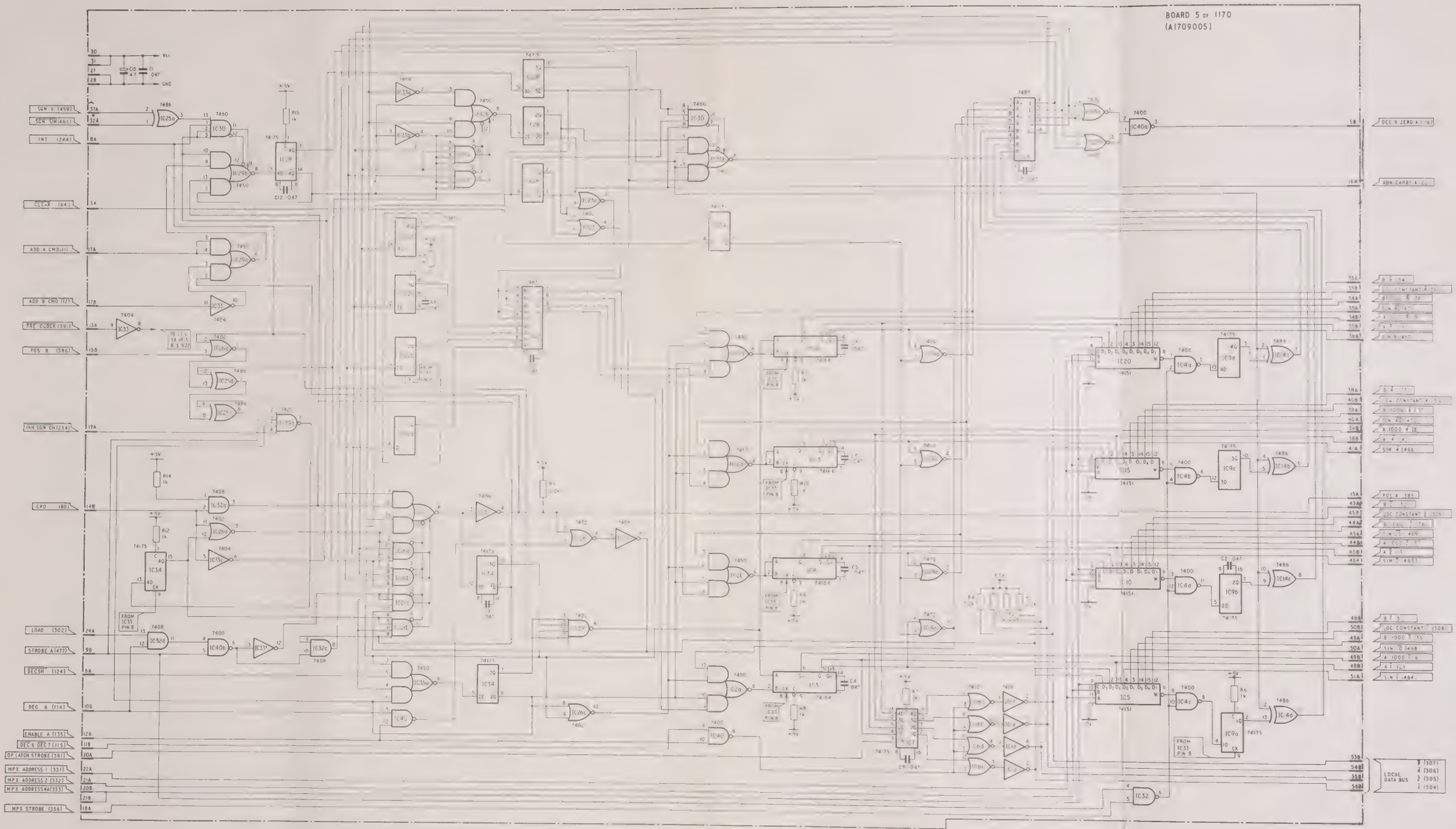
Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 55 (cont.)

SOURCE	SIG No.	DESTINATION
	5	55A
53	467	
55A	33	
54	310	
55A	37	
53	470	
	8	55A
	4	55A
53	466	
	385	56.55A
55A	32	
54	309	
55A	36	
53	469	
	7	55A
	3	55A
53	465	
55A	31	
54	308	
55A	35	
53	468	
	6	55A
	2	55A
53	464	
E	307	56.57.63.55A
E	306	56.57.63.55A
E	305	56.57.63.55A
E	304	56.57.63.55A

← Alternative list for board 5 when fitted in position 6.



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 56

SOURCE	SIG No.	DESTINATION
61	137	57
64	120	54.57
64	119	54.57
64	118	54.57
54	246	
	123	
54	254	57
	475	
	160	
62	323	20.50.52
73	312	
	488	
63	408	58
54	52	57.64
62	572	
55A	386	55
55	385	55A
	148	
55A	117	
55	116	
62	81	
63	407	58
63	405	58.62
63	404	58
63	403	58
63	402	58
61	135	55.55A
61	136	55A

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 56 (cont.)

SOURCE	SIG No.	DESTINATION
	335	54
	332	55.55A
	333	55
	334	55A
	12	55.55A
	11	55.55A
	551	57
	255	57
	590	54
	64	55
	302	54.55.55A
	493	54
	494	54
	478	55A
	477	55
	234	55.55A
E	304	55.57.63.55A
E	305	55.57.63.55A
E	306	55.57.63.55A
E	307	55.57.63.55A
	244	54.55.57.55A
	97	50
	303	57
	1	
	30	
	19	64
	20	64
	124	55.55A
	115	55.55A
	114	55.55A

BOARD 7 of 1170
(A1709007)

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

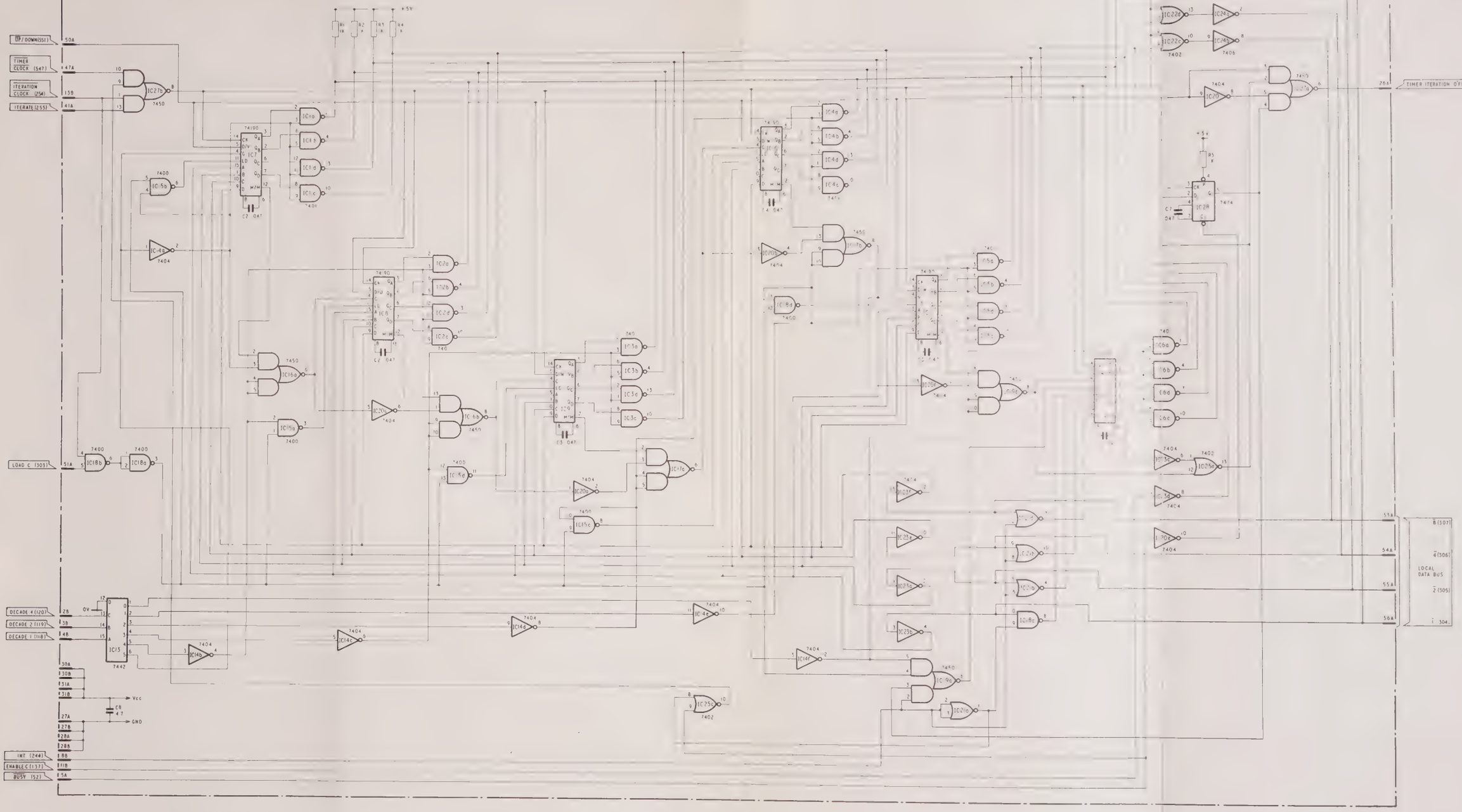
Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 57

SOURCE	SIG No.	DESTINATION
54	52	56.64
61	137	56
56	244	54.55.55A
64	118	54.56
64	119	54.56
64	120	54.56
56	303	
56	255	
54	254	56
54	547	
56	551	
	544	54
	307	55.56.63
	306	55.56.63
	305	55.56.63
	304	55.56.63

BOARD 8 OF 1170
(A1709008)



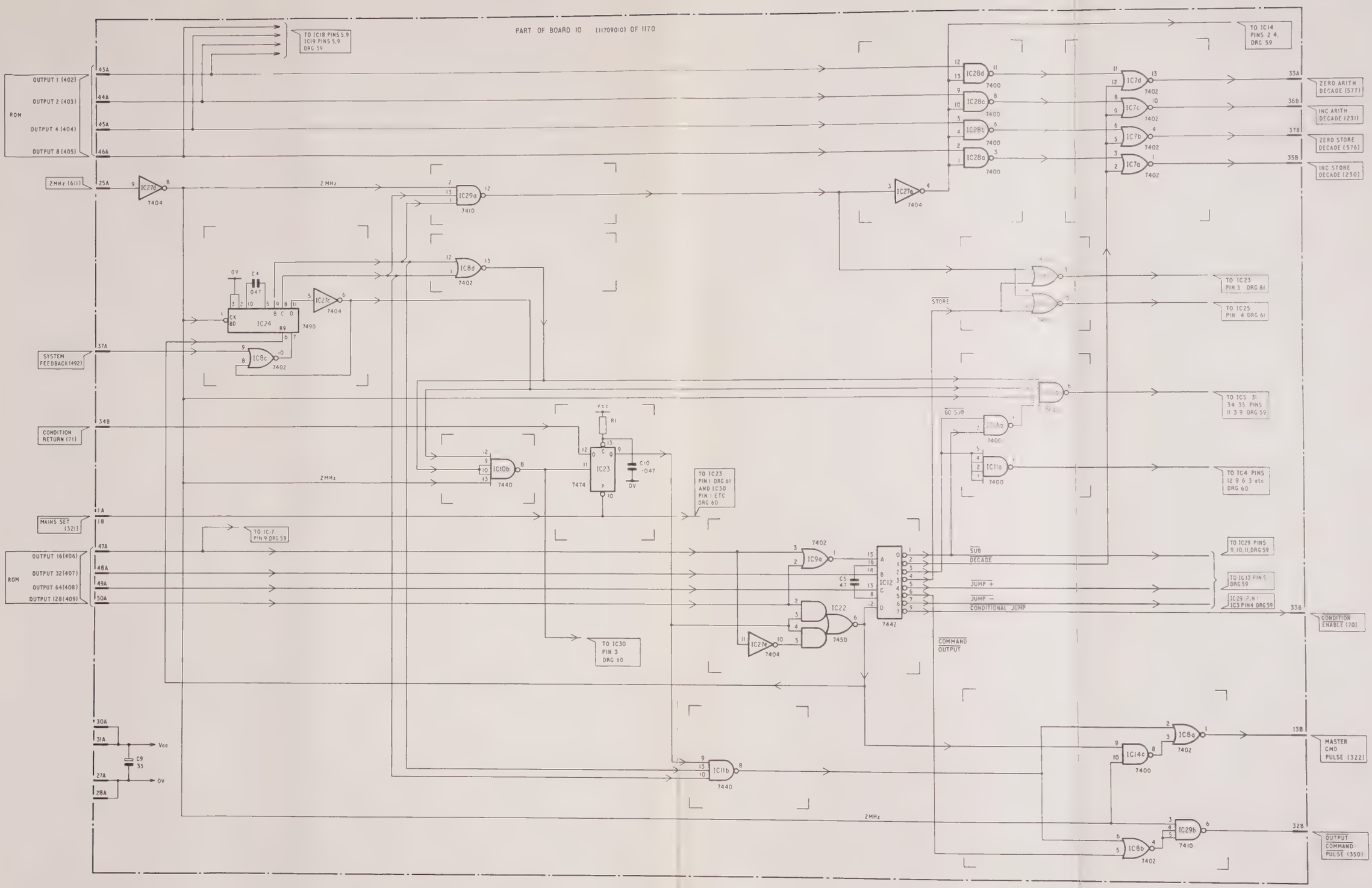
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 58

SOURCE	SIG No.	DESTINATION
63	409	
63	408	56
63	407	56
63	406	
4	321	30.34.50.66
64	71	
64	492	
2	611	21.25.50.54.65.66.69.70.72.
63	405	56.62
63	404	56
63	403	56
63	402	56
	577	64
	231	64
	576	65
	230	65
	70	64
	322	64
	350	62



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

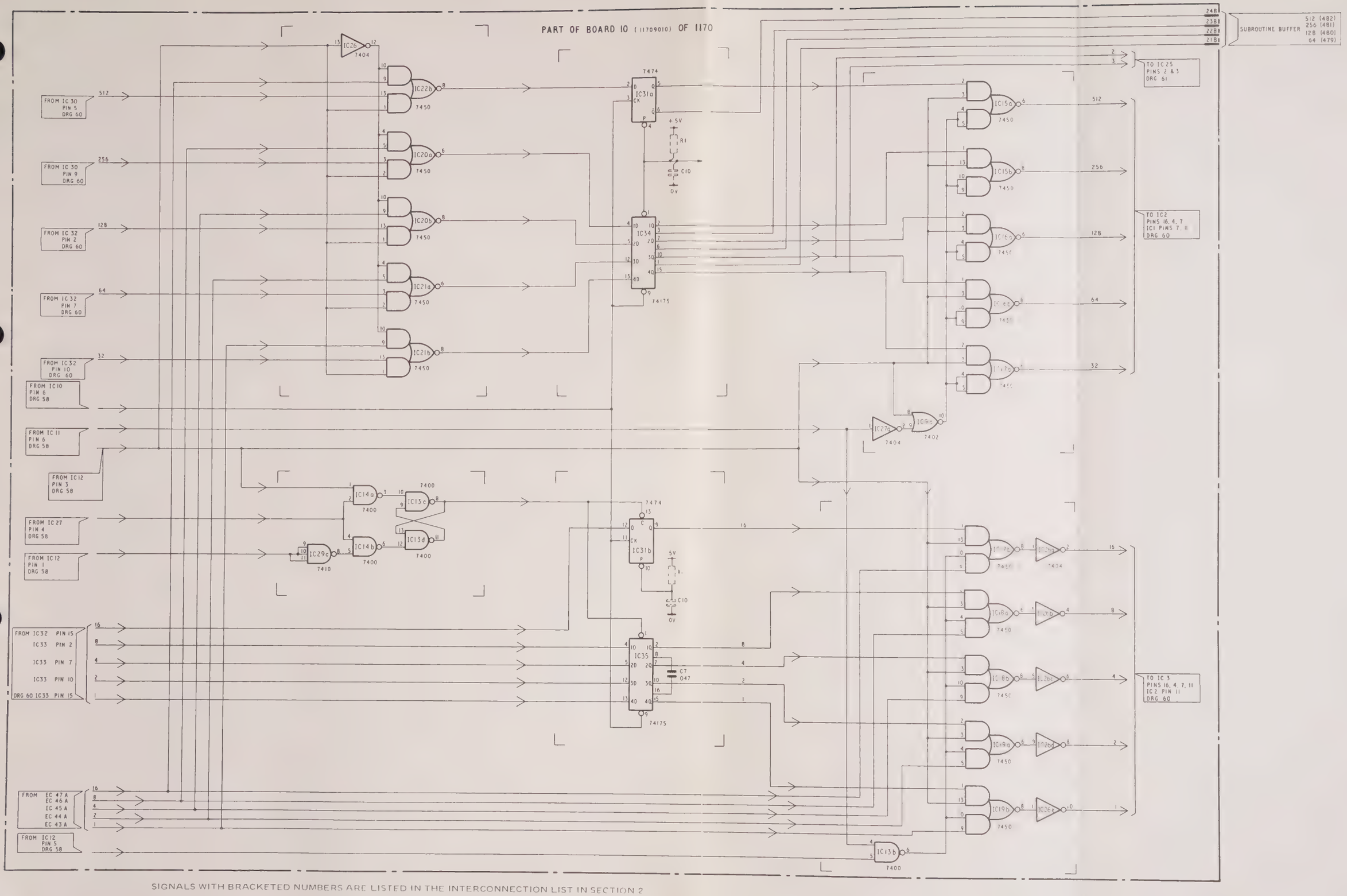
Circuit 59 See pages 1.3.28 on.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 59

SOURCE	SIG No.	DESTINATION
	482	65
	481	65
	480	65
	479	65


SUBROUTINE BUFFER
512 (482)
256 (481)
128 (480)
64 (479)
TO IC25 PINS 2 & 3 DRG 61
TO IC2 PINS 16, 4, 7, 11 IC1 PINS 7, 11 DRG 60
TO IC3 PINS 16, 4, 7, 11 IC2 PIN 11 DRG 60
FROM IC 30 PIN 5 DRG 60
FROM IC 30 PIN 9 DRG 60
FROM IC 32 PIN 2 DRG 60
FROM IC 32 PIN 7 DRG 60
FROM IC 32 PIN 10 DRG 60
FROM IC10 PIN 6 DRG 58
FROM IC11 PIN 6 DRG 58
FROM IC12 PIN 3 DRG 58
FROM IC 27 PIN 4 DRG 58
FROM IC12 PIN 1 DRG 58
FROM IC32 PIN 15
IC33 PIN 2
IC33 PIN 7
IC33 PIN 10
DRG 60 IC33 PIN 15
FROM EC 47 A
EC 46 A
EC 45 A
EC 44 A
EC 43 A
FROM IC12 PIN 5 DRG 58
7474
74175
7400
7410
7450
7404
7402
+5V
0V
C10
C7 047

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

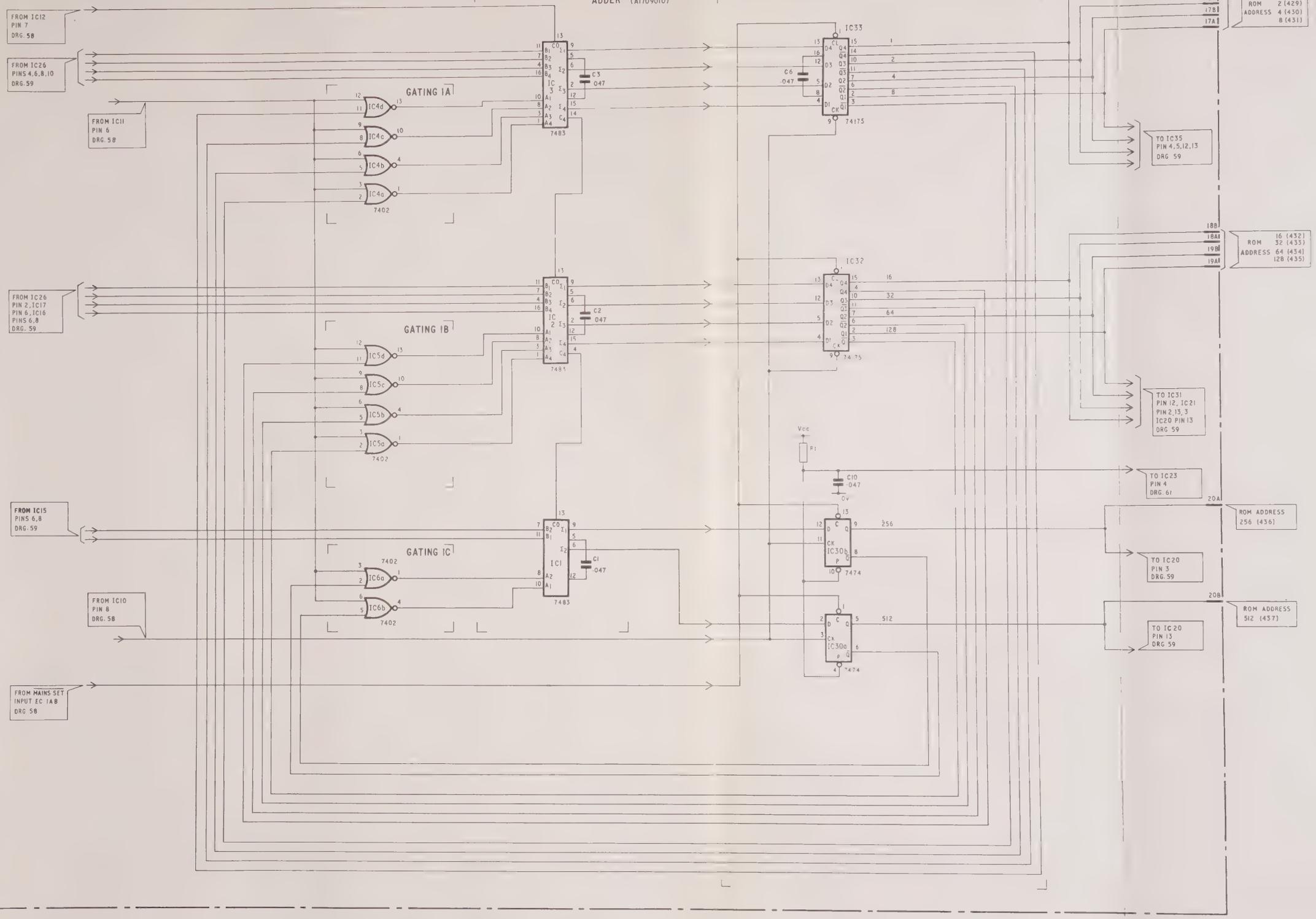
Circuit 60 See pages 1.3.28 on.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 60

SOURCE	SIG No.	DESTINATION
	428	63
	429	63
	430	63
	431	63
	432	63
	433	63
	434	63
	435	63
	436	63
	437	63



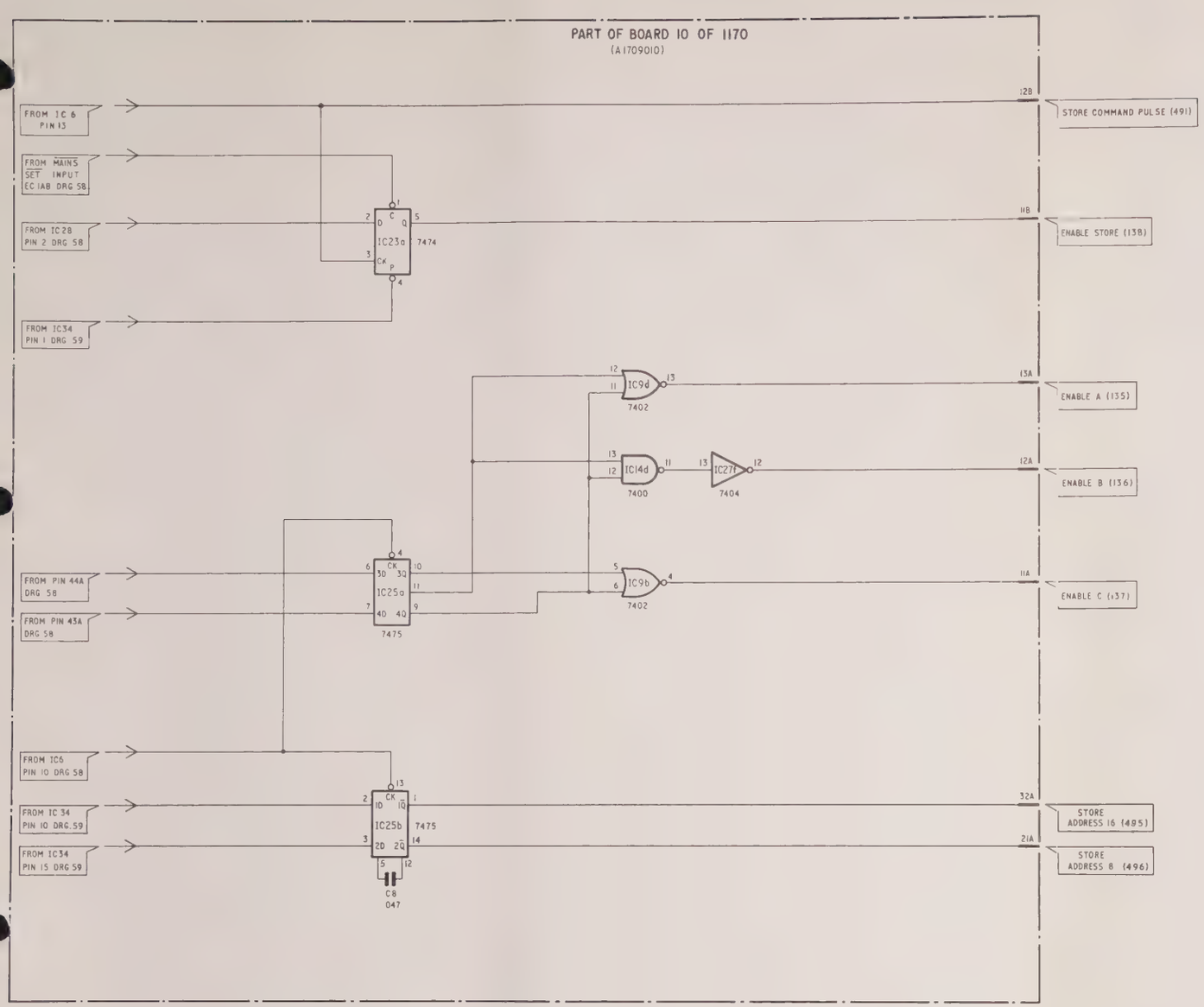
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 61

SOURCE	SIG No.	DESTINATION
	491	65
	138	64
	135	55.56.55A
	136	56.55A
	137	56.57
	495	65
	496	65



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

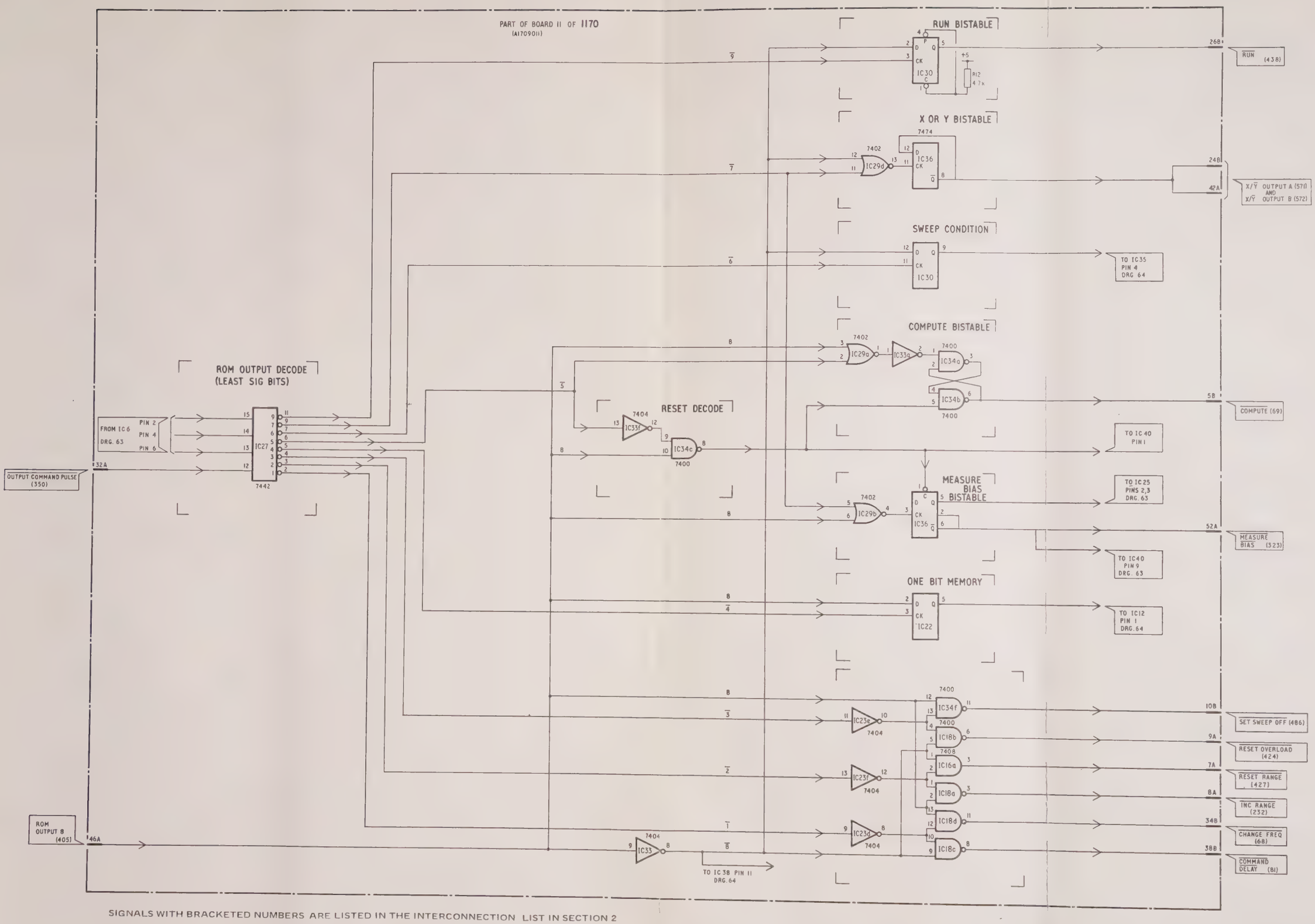
Circuit 62 See pages 1.3.28 on.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 62

SOURCE	SIG No.	DESTINATION
63	405	56.58
58	350	
	438	29.33.73
	571	19
	69	71
	323	20.50.52.56
	486	33
	424	73
	427	73
	232	73
	68	70
	81	56



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 63

SOURCE	SIG No.	DESTINATION
60	436	
60	437	
60	435	
60	434	
60	433	
60	432	
60	431	
60	430	
60	429	
60	428	
66	342	3.50.70.71.72.74
66	341	3.50.70.71.72.73.74
66	340	3.50.70.71.72.74
66	339	3.50.69.70.71.72.74
73	243	20
73	242	20
	50	24
	51	24
70.71	343	66
70.71	344	66
70.71	345	66
70.71	346	66
E	304	55.56.57
E	305	55.56.57
E	306	55.56.57
E	307	55.56.57
	402	56.58
	403	56.58
	404	56.58
	405	56.58.62
	406	58
	407	56.58
	408	56.58
	409	58

PART OF BOARD II (A170901) OF 1170

INPUT RANGE 2 (242)
INPUT RANGE 4 (243)
MOS STORE DATA OUTPUT 1 (339)
OUTPUT 2 (340)
OUTPUT 4 (341)
OUTPUT 8 (342)
FROM IC9 PINS 12,9 4,7 DRG 65
FROM IC5 PIN 10 DRG 64
FROM IC2 PIN 8 DRG 64
FROM IC12 PIN 8 DRG 65 AND IC21 PIN 1 DRG 64
TO IC17 PIN 2 DRG 64
FROM IC36 PIN 5 DRG 62
FROM IC20 PIN 6 DRG 64
BIAS RANGE A (50)
BIAS RANGE B (51)
MOS STORE DATA INPUT 1 (343)
INPUT 2 (344)
INPUT 4 (345)
INPUT 8 (346)
LOCAL DATA BUS 1 (304)
BUS 2 (305)
BUS 4 (306)
BUS 8 (307)
ROM ADDRESS 1 (428)
2 (429)
4 (430)
8 (431)
16 (432)
32 (433)
64 (434)
128 (435)
ROM ADDRESS 512 (437)
ROM ADDRESS 256 (436)
ROM OUTPUT 1 (402)
OUTPUT 2 (403)
OUTPUT 4 (404)
OUTPUT 8 (405)
OUTPUT 16 (406)
OUTPUT 32 (407)
OUTPUT 64 (408)
OUTPUT 128 (409)

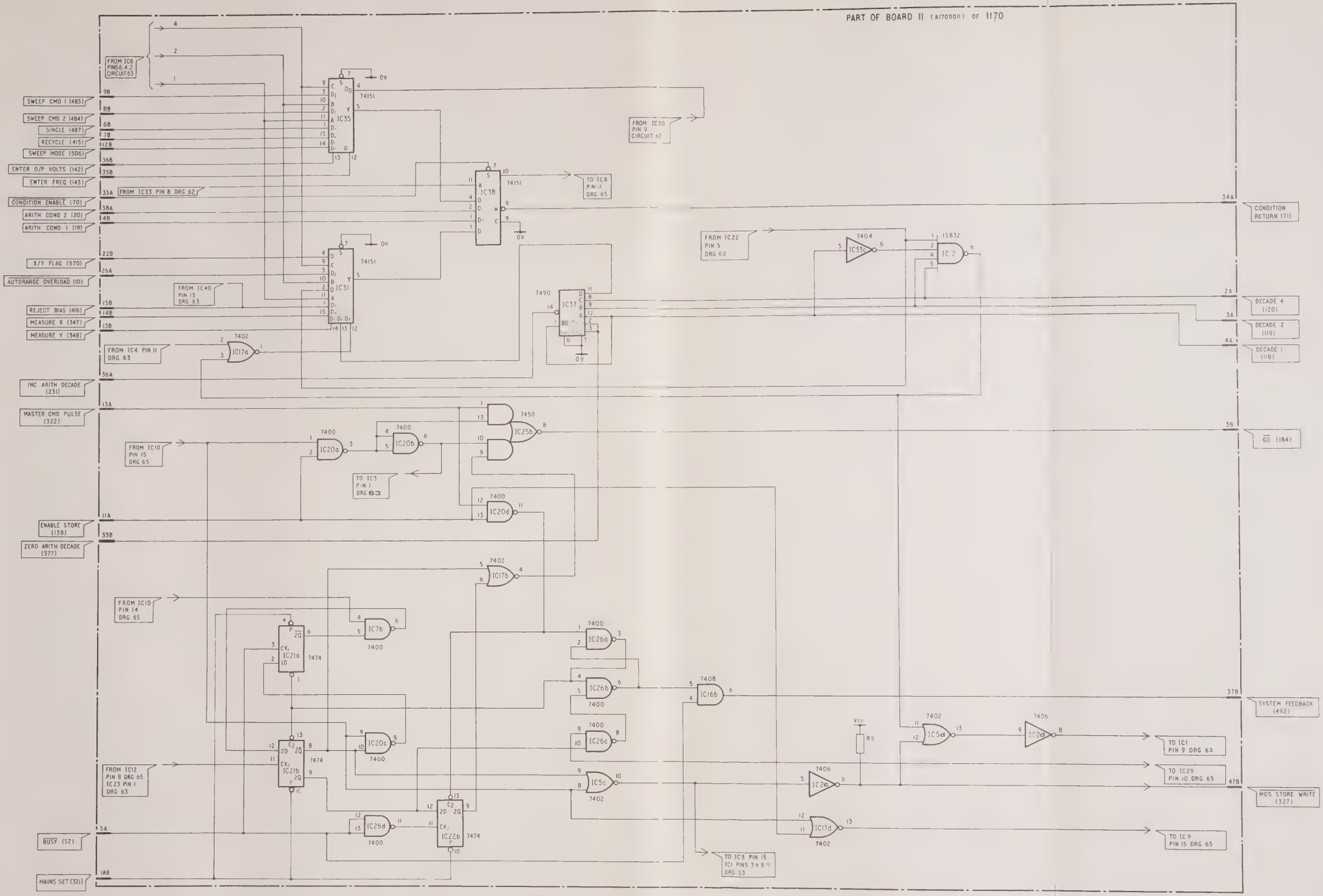
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 64

SOURCE	SIG No.	DESTINATION
54	52	56.57
58	577	
61	138	
58	322	
58	231	
32	348	69.71
32	347	69.71
34	416	
73	10	50
19	570	
56	19	
56	20	
58	70	
67	143	
67	142	
33	506	70
33	415	
33	487	
33	484	
33	483	
	71	58
54	120	56.57
54	119	56.57
54	118	56.57
	184	54
	492	58
70	327	66



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

1170 MAIN CONTROL 'B' (2)

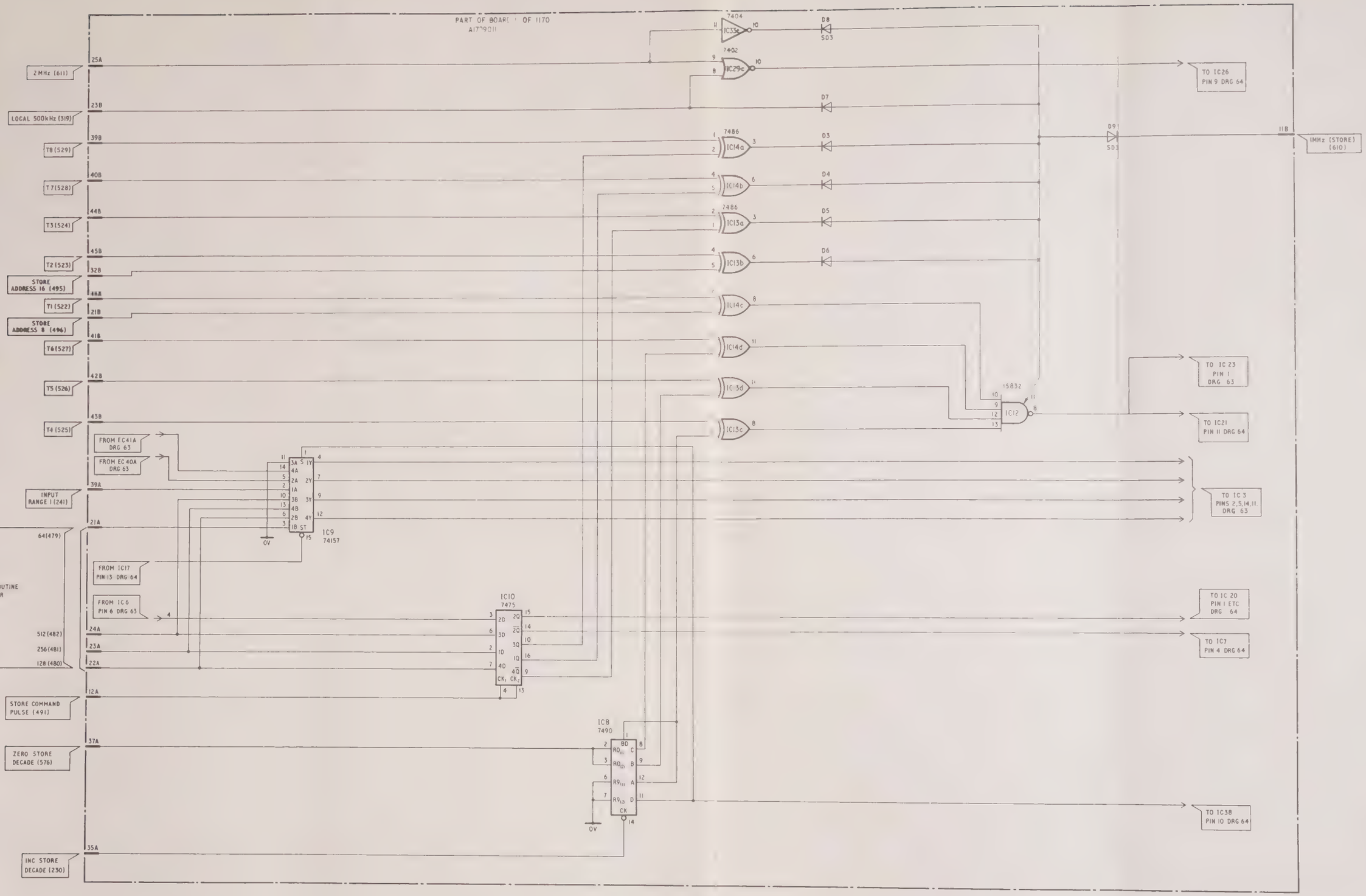
11707064 - C

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 65

SOURCE	SIG No.	DESTINATION
58	230	
58	576	
61	491	
59	480	
59	481	
59	482	
59	479	
73	241	20
67	525	69
67	526	69
67	527	69
61	496	
67	522	69
61	495	
67	523	69
67	524	69
67	528	69
67	529	69
66	319	69
2	611	21.25.50.54.58.66.69.70.72
66	610	



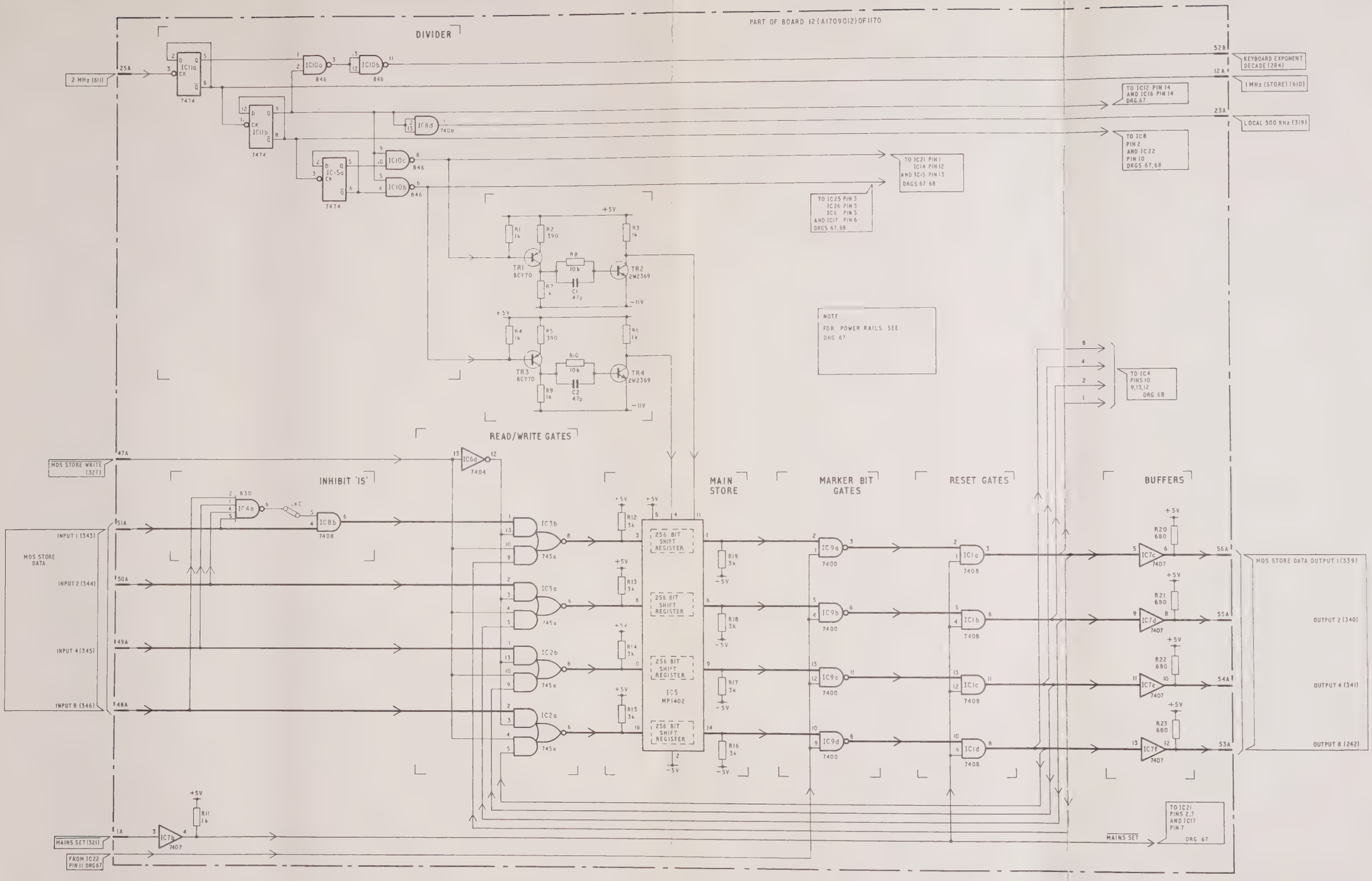
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 66

SOURCE	SIG No.	DESTINATION
4	321	30.34.50.58
63.70.71	346	
63.70.71	345	
63.70.71	344	
63.70.71	343	
64.70	327	
2	611	21.25.50.54.58.65.69.70.72
70	284	71
65	610	
	319	65.69
	339	3.50.63.69.70.71.72.74
	340	3.50.63.70.71.72.74
	341	3.50.63.70.71.72.73.74
	342	3.50.63.70.71.72.74



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 67

SOURCE	SIG No.	DESTINATION
70	166	
70	140	
70	139	71
70	554	
	522	65.69
	523	65.69
	524	65.69
	525	65.69
	526	65.69
	527	65.69
	528	65.69
	529	65.69
	542	3.69
	543	3.69
	538	69
	539	69
	540	69
	142	64
	143	64

PART OF BOARD 12 (A1709012) OF 1170

MAIN SET DELAY

FROM IC10 PIN 6 SEE DRG 66

FROM IC13 PIN 3 SEE DRG 68

FROM IC11 PIN 9 SEE DRG 66

IC17b

R27 1k

IC27b

TO IC25 PIN 4 SEE DRG 68

30A
30B — +5V → +5V TO: PIN 14 ON ICs 1-4, 6-11, 13-15, 20, 21-23, 25-32; PIN 5 ON ICs 5, 17-19, 21, 24; PIN 16 ON ICs 12, 16
31A
31B

27A
28A — 0V → 0V TO: PIN 7 ON ICs 1-4, 6-11, 13-15, 20, 21-23, 25-32; PIN 13 ON ICs 17-19, 21, 24; PIN 8 ON ICs 12, 16

R26 10K

−5V → TO IC5 PIN 12

DZ 5.6V

11A — −11V

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

TIMING COUNTER

7408 IC20a

IC12 74191 — (1) (2) (4) (8) → 46A T1 (522), 45A T2 (523), 44A T3 (524), 43A T4 (525)

IC16 74191 — (16) (32) (64) (128) → 42A T5 (526), 41A T6 (527), 40A T7 (528), 39A T8 (529)

IC8c 7408

TO IC13 PIN 4 SEE DRG 68

IC19a 7476 — (256) → T9 → 34A; T9 → TO IC23 PINS 4 AND 1 ETC SEE DRG. 68

IC19b 7476 — (512) → T10 → 33A; T10 → TO IC23 PINS 13 AND 9 ETC SEE DRG 68

IC18a 7476 — (1024) → T11 → 37A

IC20c 7408; IC18b 7476 — (2048) → T12 → 36A

IC20b 7408; IC7a 7476 — (4096) → T13 → 35A

34A T9 (DIGIT CONTROL) (542); 33A T10 (DIGIT CONTROL) (543)

37A T11 (EQUIV TIMING) (538); 36A T12 (EQUIV TIMING) (539); 35A T13 (EQUIV TIMING) (540)

32B ENTER O/P VOLTS (142)

32A ENTER FREQ (143)

38B VOLTS (KEYBOARD) (554)
5B ENTER PULSE (139)
52A END OF ENTER (140)
38A FREQ (KEYBOARD) (166)

IC30 7402; IC31 7400

MARKER BIT GENERATOR

FROM IC11 PIN 8 SEE DRG 66

FROM IC10 PIN 8 SEE DRG 66

FROM IC7 PIN 4 SEE DRG 66

IC8a 7408; IC21a 7476; IC28d 7408; IC21b 7476; IC22d 7400

TO IC9 PIN 9 ETC SEE DRG 66

TIMING COUNTER & MARKER BIT GENERATOR

67

D11707067-02

Circuit 68 See pages 1.3.28 on.

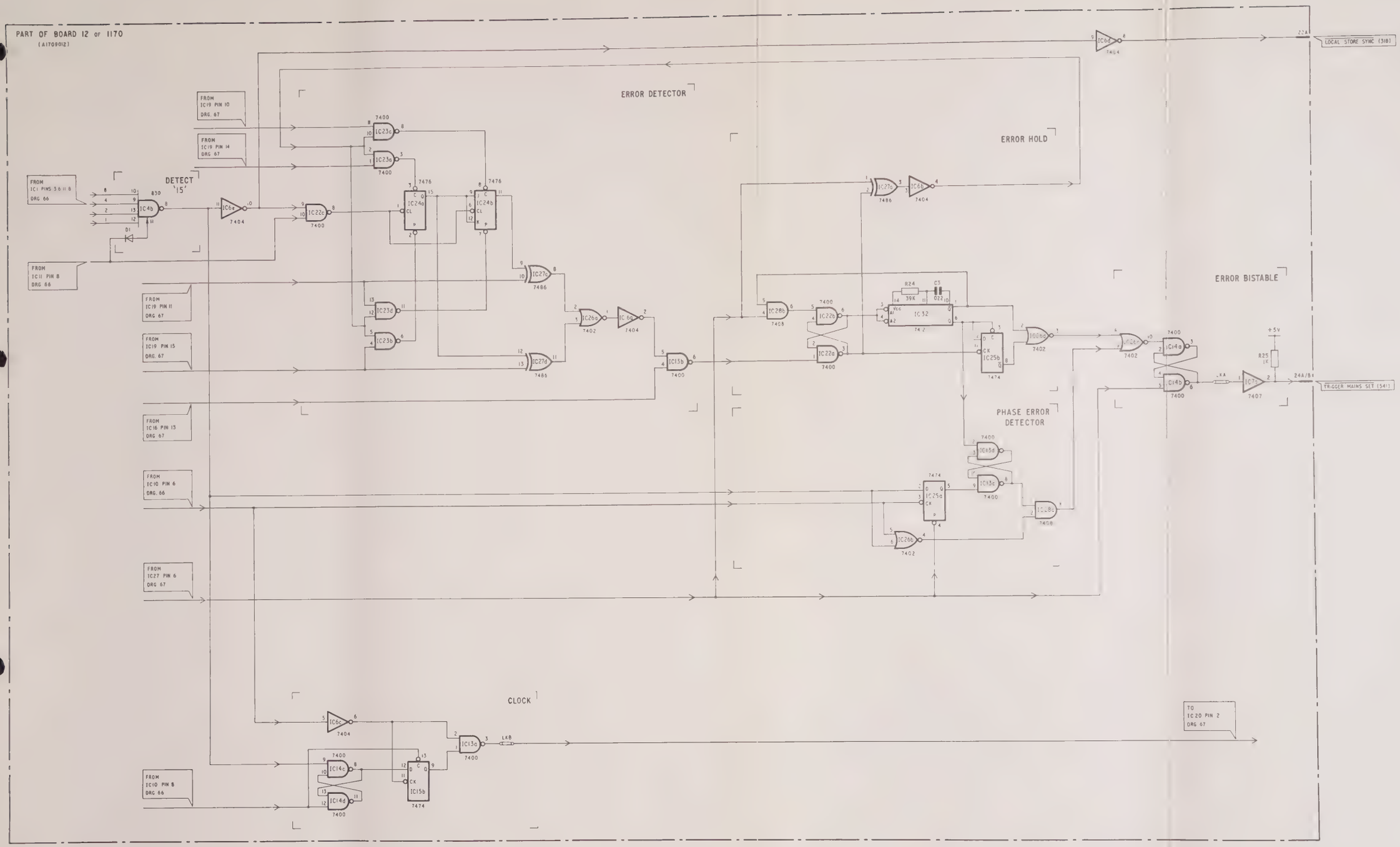
Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 68

SOURCE	SIG No.	DESTINATION
	318	69
	541	44

PART OF BOARD 12 OF 1170
(A1709012)



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

ERROR DETECTION LOGIC
BOARD 12

D11707068 - 02

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 69

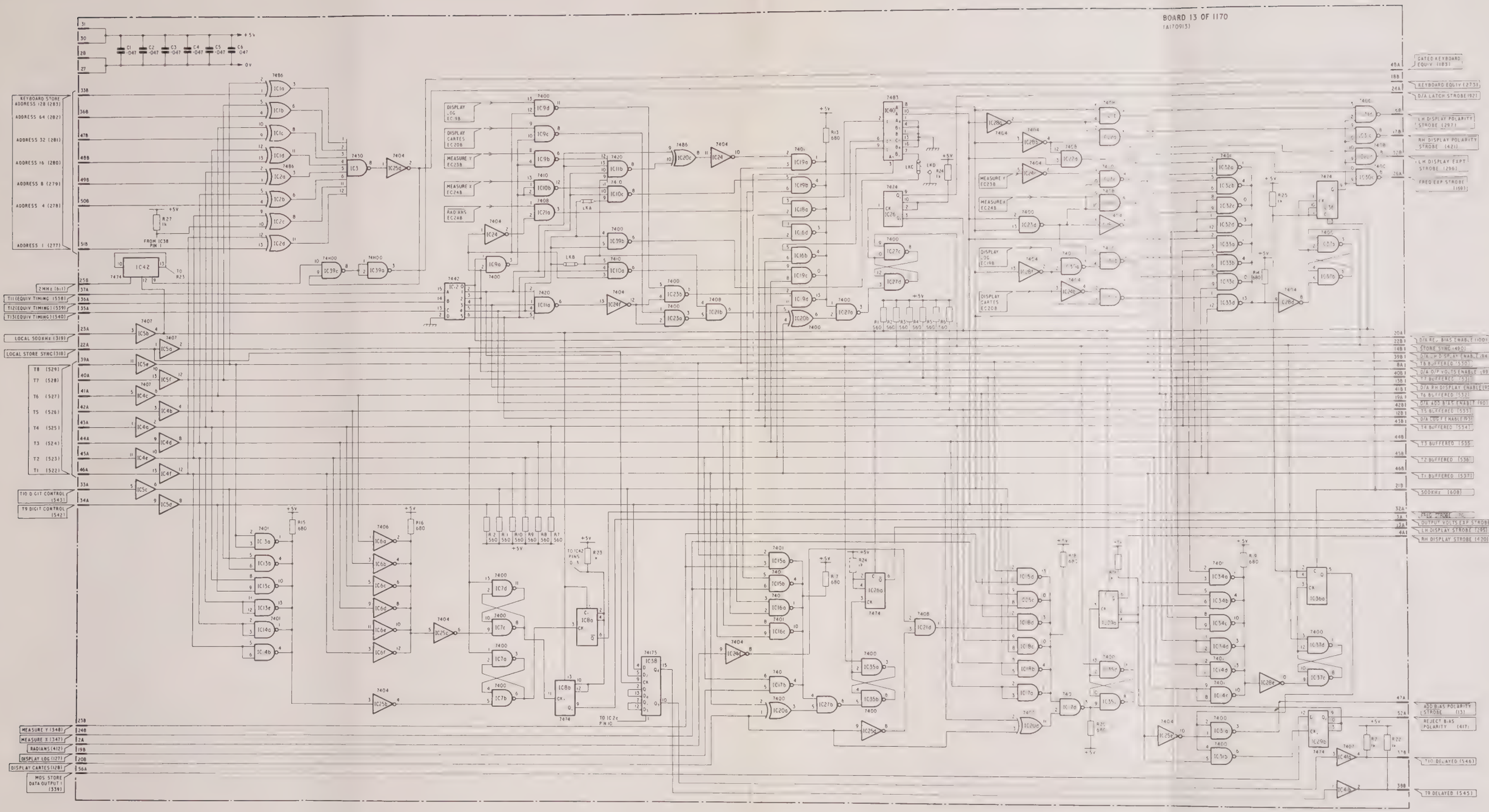
SOURCE	SIG No.	DESTINATION
66	339	3.50.63.70.71.72.74
32	128	71.74
32	127	71
	412	74
32	347	64.71
32	348	64.71
67	542	3
67	543	3
67	522	65
67	523	65
67	524	65
67	525	65
67	526	65
67	527	65
67	528	65
67	529	65
68	318	
66	319	65
67	540	
67	539	
67	538	
2	611	21.25.50.54.58.65.66.70.72
70	277	
70	278	
70	279	
70	280	
70	281	
70	282	
70	283	
	183	70
	273	70
	92	72

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 69 (cont.)

SOURCE	SIG No.	DESTINATION
	297	71.73
	421	71
	296	71
	169	50
	100	72
	490	70.72.74
	94	72
	530	31
	99	72
	531	31
	95	72
	532	31
	90	72
	533	31
	93	72
	534	31
	535	31
	536	31
	537	31
	608	30
	170	3
	358	3
	295	74
	420	74
	13	3
	417	23
	546	70.71.72.75
	545	70.71.72.75


BOARD 13 OF 1170
(A170913)
KEYBOARD STORE ADDRESS 128 (283)
ADDRESS 64 (282)
ADDRESS 32 (281)
ADDRESS 16 (280)
ADDRESS 8 (279)
ADDRESS 4 (278)
ADDRESS 1 (277)
2 MHz (611)
T11 (EQUIV TIMING) (538)
T12 (EQUIV TIMING) (539)
T13 (EQUIV TIMING) (540)
LOCAL 500KHz (319)
LOCAL STORE SYNC (318)
T8 (529)
T7 (528)
T6 (527)
T5 (526)
T4 (525)
T3 (524)
T2 (523)
T1 (522)
T10 DIGIT CONTROL (543)
T9 DIGIT CONTROL (542)
MEASURE Y (348)
MEASURE X (347)
RADIANS (412)
DISPLAY LOG (127)
DISPLAY CARTES (128)
MOS STORE DATA OUTPUT (539)
DISPLAY LOG EC19B
DISPLAY CARTES EC20B
MEASURE Y EC23B
MEASURE X EC24B
RADIANS EC24B
GATED KEYBOARD EQUIV (883)
KEYBOARD EQUIV (273)
D/A LATCH STROBE (921)
LH DISPLAY POLARITY STROBE (297)
RH DISPLAY POLARITY STROBE (421)
LH DISPLAY EXPT STROBE (296)
FREQ EXP STROBE (1093)
D/A RE-, BIAS ENABLE (100)
STORE SYNC (490)
D/A LH DISPLAY ENABLE (94)
T8 BUFFERED (550)
D/A D/P VOLTS ENABLE (99)
T7 BUFFERED (551)
D/A RH DISPLAY ENABLE (95)
T6 BUFFERED (552)
D/A ADD BIAS ENABLE (90)
T5 BUFFERED (553)
D/A OUTPUT ENABLE (93)
T4 BUFFERED (554)
T3 BUFFERED (555)
T2 BUFFERED (556)
T1 BUFFERED (557)
500KHz (608)
OUTPUT VOLTS EXP STROBE (558)
LH DISPLAY STROBE (295)
RH DISPLAY STROBE (420)
ADD BIAS POLARITY STROBE (13)
REJECT BIAS POLARITY (417)
T10 DELAYED (546)
T9 DELAYED (545)
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 70 See page 1.3.28

This circuit controls the display of data commanded from the Keyboard (the extreme right-hand display) and the entry of the data into the MOS store.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 70

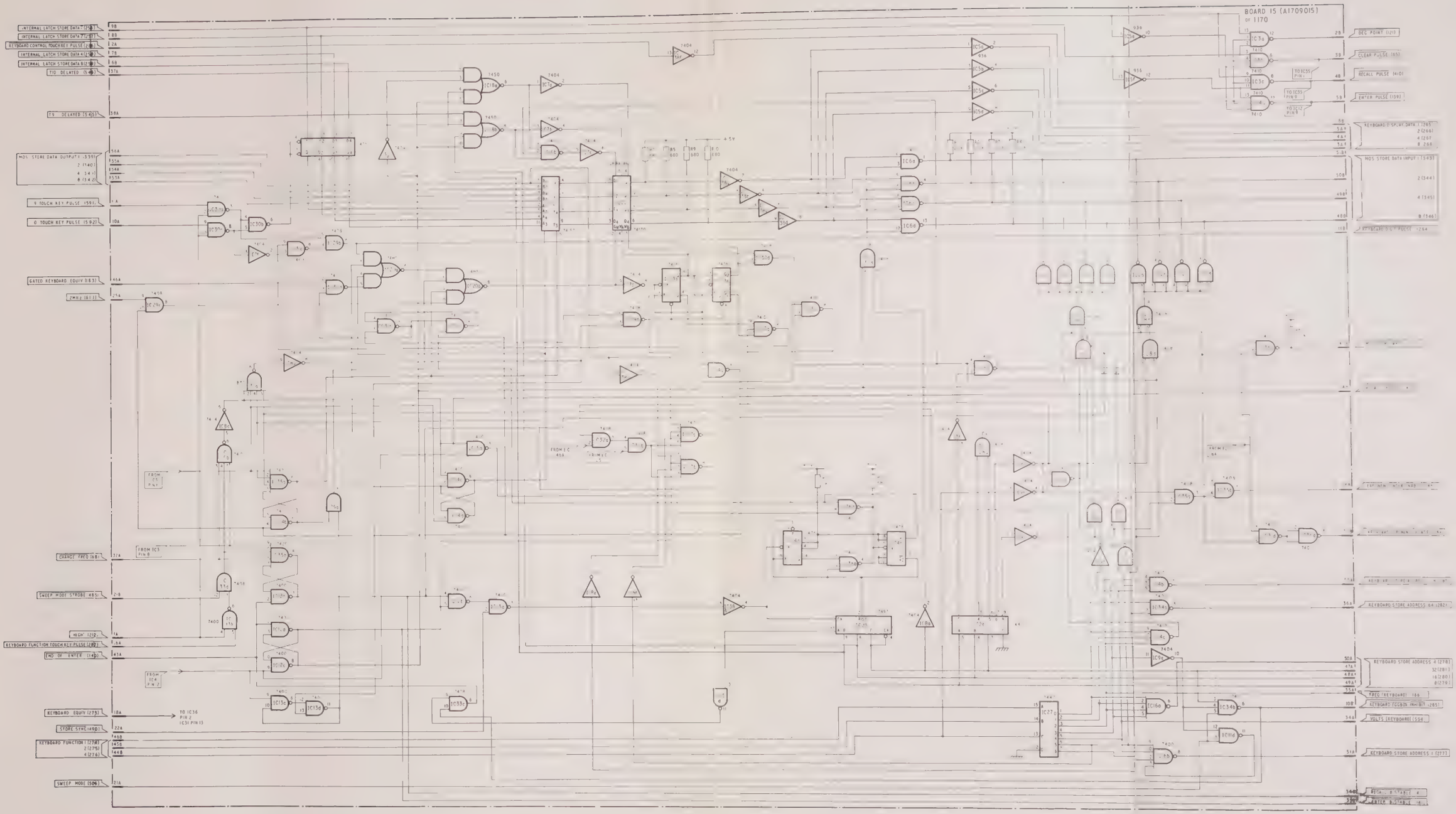
SOURCE	SIG No.	DESTINATION
33	506	64
36.71	276	
36.71	275	
36.71	274	
69	490	72.74
69	273	
36	287	70.71
31	212	36.71
36.71	485	
62	68	
2	611	21.25.50.54.58.65.66.69.72
69	183	
31	592	
31	591	
66	342	3.50.63.71.72.74
66	341	3.50.63.71.72.73.74
66	340	3.50.63.71.72.74
66	339	3.50.63.69.71.72.74
69	545	71.72.75
69	546	71.72.75
31	259	73
31	258	36.71.73
31	286	
31	257	36.71.73
31	256	36.71.73
	121	71
	65	71
	410	71

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 70 (cont.)

SOURCE	SIG No.	DESTINATION
	139	67.71
	265	75
	266	75
	267	75
	268	75
63.71	343	66
63.71	344	66
63.71	345	66
63.71	346	66
	264	71
64	327	66
	410	71
	146	71
	140	67
66	284	71
	283	69
	282	69
	278	69
	281	69
	280	69
	279	69
	166	67
	285	71
	554	67
	277	69
	411	71
	141	71



SIGNALS WITH BRACKETED NUMBERS
ARE LISTED IN THE INTERCONNECTION
LIST IN SECTION 2

Circuit 71 See page 1.3.28

This circuit controls the display of data commanded from the Keyboard (the extreme right-hand display) and the entry of the data into the MOS store.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 71

SOURCE	SIG No.	DESTINATION
36	288	
31	212	36.70
33	313	36
36	287	
31	258	36.70.73
31	257	36.70.73
31	256	36.70.73
32	128	69.74
69	297	73
69	421	
66.70	284	
70	411	
70	141	
70	264	
70	121	
	618	
35	172	
35	171	
70	146	
35	173	
70	65	
70	285	
66	342	3.50.63.70.72.74
66	341	3.50.63.70.72.73.74
66	340	3.50.63.70.72.74
66	339	3.50.63.69.70.72.74
70	139	67
72	252	
70	410	
62	69	
69	546	70.72.75
69	545	70.72.75

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 71 (cont.)

SOURCE	SIG No.	DESTINATION
69	296	
32	127	69
32	348	64.69
32	347	64.69
	298	74
	299	74
	300	74
	301	74
	553	74
	328	74
	330	74
	213	74
	289	74
	269	75
	270	75
	271	75
	272	75
63.70	343	66
63.70	344	66
63.70	345	66
63.70	346	66
36	274	70
36	275	70
36	276	70
36	485	70
36.73	290	37
36.73	291	37
36.73	292	37

BOARD 16 OF 1170
(A1709016)

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Circuit 72 See page 1.3.28

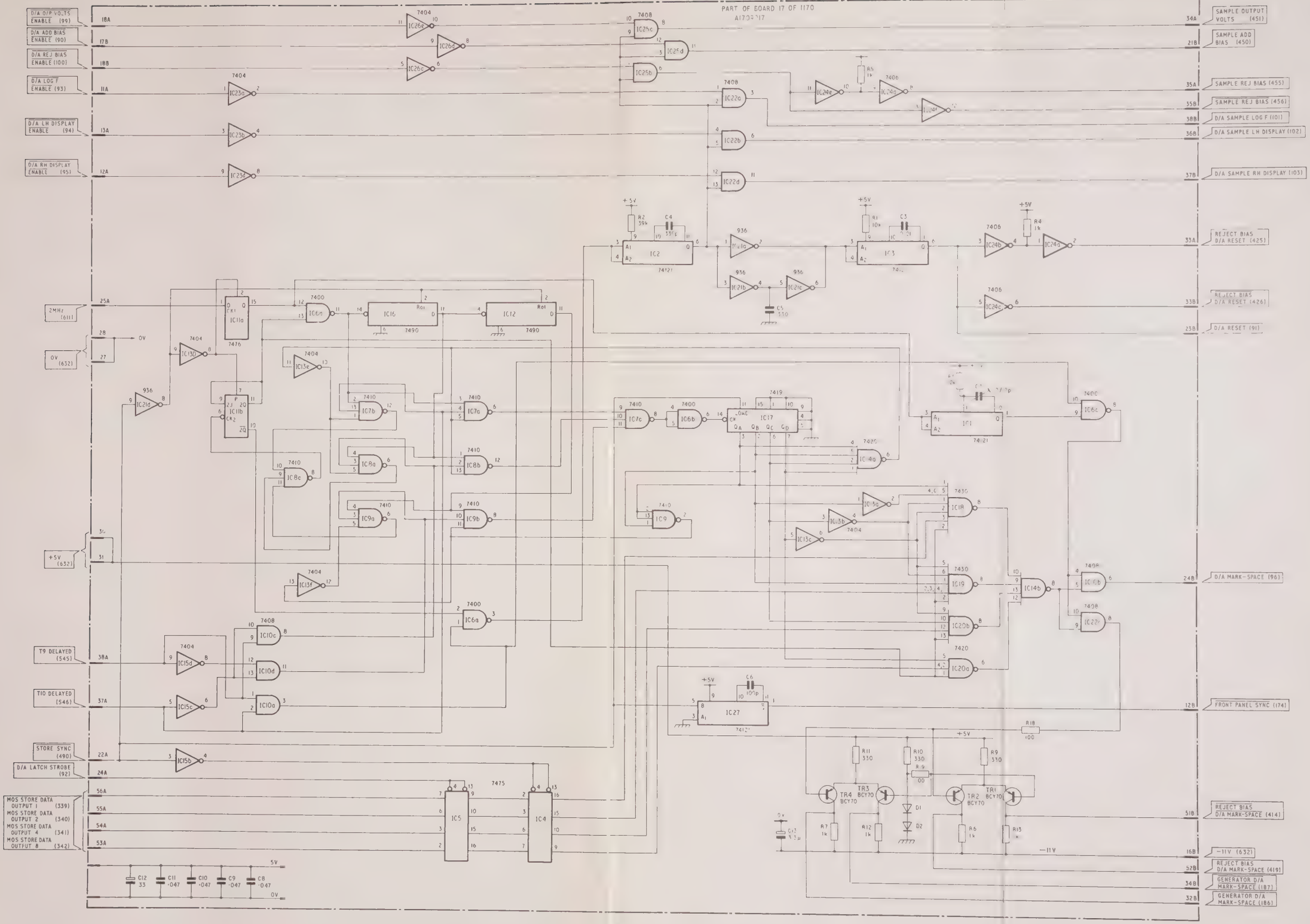
This circuit generates the D/A mark/space pulse trains, the use of which is described on page 1.3.12.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 72

SOURCE	SIG No.	DESTINATION
66	342	3.50.63.70.71.74.
66	341	3.50.63.70.71.73.74.
66	340	3.50.63.70.71.74.
66	339	3.50.63.69.70.71.74.
69	92	
69	490	70.74.
69	546	70.71.75.
69	545	70.71.75.
46.48	632	74.75.
2	611	21.25.50.54.58.65.66.69.70.
69	95	
69	94	
69	93	
69	100	
69	90	
69	99	
	451	12
	450	12
	455	22
	456	22
	101	
	102	
	103	
	425	22
	426	22
	91	12
	96	
	174	25.30
	414	22
	419	22
	187	12
	186	12



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2.

Circuit 73 See page 1.3.28

This circuit controls the Auto ranging and overload indicator system.

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 73

SOURCE	SIG No.	DESTINATION
69	297	71
66	341	3.50.63.70.71.72.74.
33	122	
2	598	
62	424	
21	260	
62	427	
62	232	
31	17	
31	259	70
31	258	36.70.71.
31	257	36.70.71.
31	256	36.70.71.
62	438	29.33.
31	253	
31	240	
31	355	
36.71	290	37
36.71	291	37
36.71	292	37
	293	37
	241	20.65
	242	20.63
	243	20.63
	10	50.64
	312	56
	252	71

PART OF BOARD 17
(A1709017) OF 1170

OVERLOAD LATCH READ STROBE (355) 14A
INPUT RANGE LATCH READ STROBE (240) 3A
INPUT RANGE TOUCH KEY PULSE (255) 5A
RUN (438) 26A
INTERNAL LATCH STORE DATA 1 (256) 9A
2 (257) 8A
4 (258) 7A
8 (259) 6A
AUTORANGE LATCH READ STROBE (17) 4A
INC RANGE (232) 8B
RESET RANGE (427) 7B

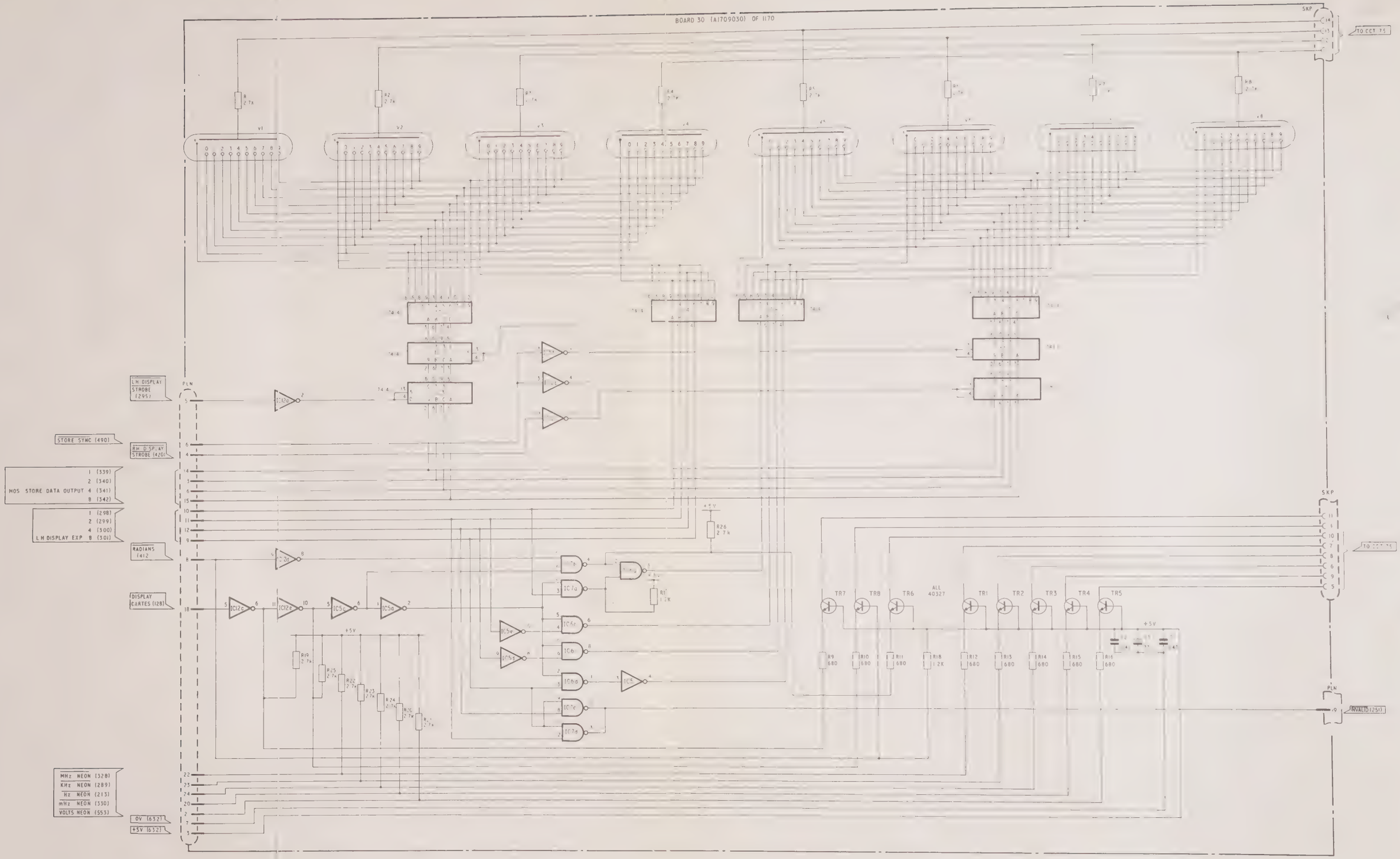
+5V
R14 1k
7406 IC34d
IC34c
IC34f
IC29a
IC29b
7401 IC29d
IC29c
42A LATCH STORE DATA OUTPUT 1 (290)
41A LATCH STORE DATA OUTPUT 2 (291)
40A LATCH STORE DATA OUTPUT 4 (292)
39A LATCH STORE DATA OUTPUT 8 (293)
IC33 7475
7457 IC35
IC24 7490
7400 IC32a
7404 IC31f
IC31d
IC31e
IC32d
IC32b
IC32c
IC35a
IC35b
IC35c
IC35d
R 43A INPUT RANGE 1 (241)
Q 44A INPUT RANGE 2 (242)
P 45A INPUT RANGE 4 (243)

INPUT OVERLOAD (260) 2B
RESET OVERLOAD (424) 9B
IC37a IC37b 7400
32A AUTORANGE OVERLOAD (10)
6B LATCHED OVERLOAD (312)

10Hz (598) 15A
R8 47
C14 150p
TO PIN 7 IC38
IC38b 7474
IC37d IC37c 7400
IC31e 7404
IC38c
21A INDICATE OVERLOAD (252)

DISABLE DISPLAY (122) 17A
MOS STORE DATA OUTPUT 4 (341) 54A
LH DISPLAY POLARITY STROBE (297) 16A
IC38a 7474

SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2



SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 74

SOURCE	SIG No.	DESTINATION
46	632	72.75
71	553	
71	330	
71	213	
71	289	
71	328	
32	128	69.71.
	412	69
71	301	
71	300	
71	299	
71	298	
66	342	3.50.63.70.71.72.
66	341	3.50.63.70.71.72.73.
66	340	3.50.63.70.71.72.
66	339	3.50.63.69.70.71.72.
69	420	
69	490	70.72
69	295	
34	251	75

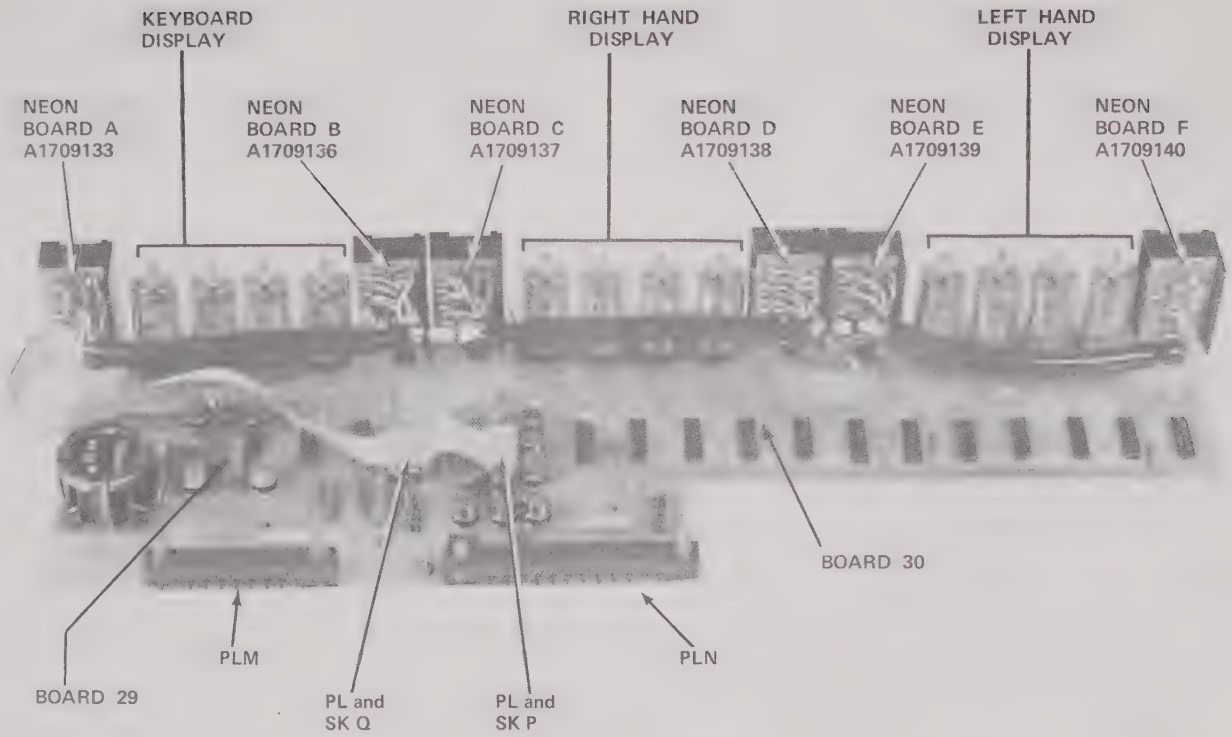
The Display Unit Circuits 74 and 75

This is a detachable assembly consisting of pcbs 29, 30 and Neon boards A to F.

The display consists of three banks of four numerical indicator tubes and six stacks of Neon lamps (Eggboxes).

All indicators are supplied from a 160V inverter and carried on four time-shared lines. The inverter consists of TR4, TR5 and associated circuitry. Time-sharing of the four lines is controlled by input lines T9 and T10 delayed (545, 546).

The rest of the circuitry of the display unit is used to decode the signals from the digital section. The required combination of high voltage on the diode and zero on the cathode illuminates the correct combinations of indicators. As this is a time-shared operation only certain combinations of indicators may be illuminated at a time. The sequential and repetative scanning of the correct indications form the apparently steady display.



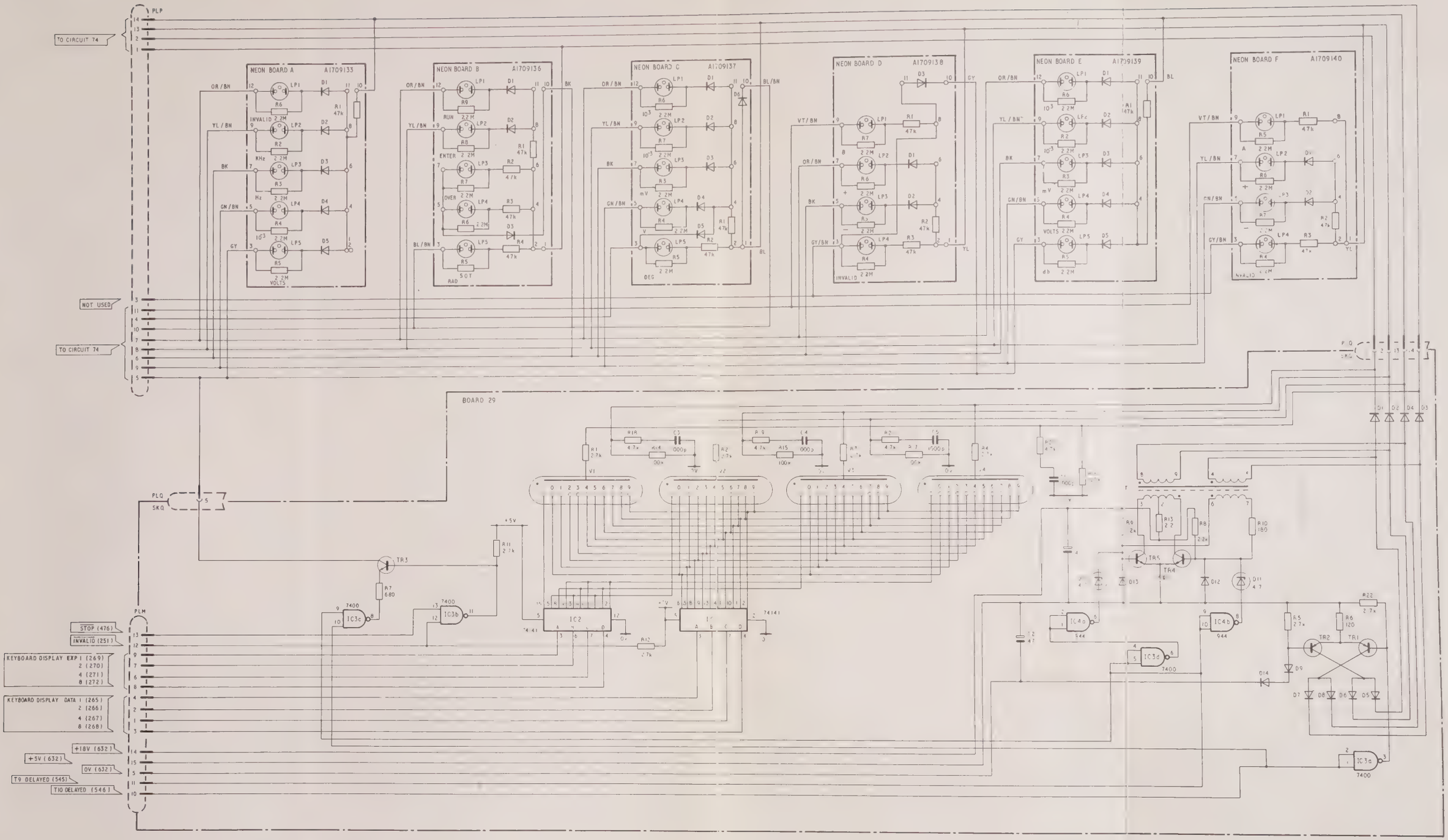
DISPLAY ASSEMBLY CIRCUIT 75

Interconnections

Signal numbers are as in Section 2.4.
Sources and destinations are circuit diagram numbers; if none shown all connections are within this circuit.

CIRCUIT No. 75

SOURCE	SIG No.	DESTINATION
69	546	70.71.72.
69	545	70.71.72.
46.47.48	632	72.74.
70	268	
70	267	
70	266	
70	265	
71	272	
71	271	
71	270	
71	269	
34.74	251	
33	476	50



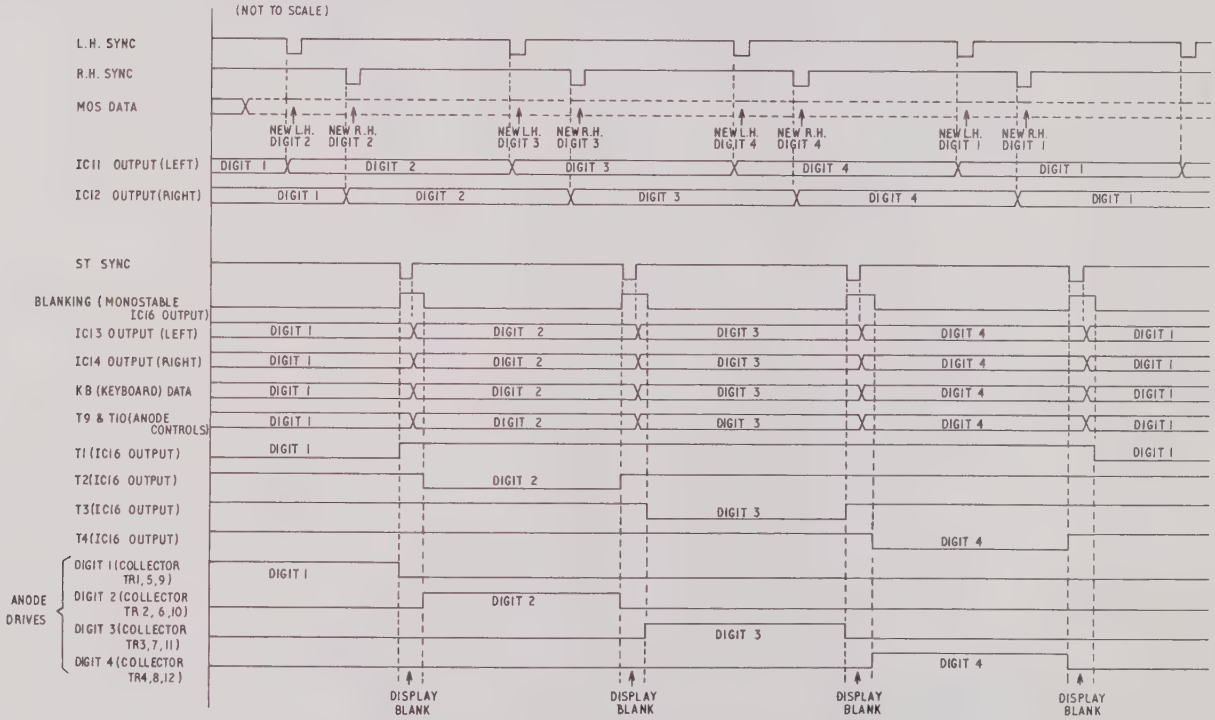
SIGNALS WITH BRACKETED NUMBERS ARE LISTED IN THE INTERCONNECTION LIST IN SECTION 2

LED Display Assembly: PCB 49 and 50

The circuit diagrams for pcb's 49 and 50 are shown in circuits 76 and 77 respectively. The pcb's are physically interconnected by means of Berg connectors. These connectors are drawn in a row on both circuit diagrams; the actual order of their physical layout is illustrated at the bottom of circuit 77.

Pcb 49 contains decoding logic, latches and a monostable. Pcb 50 contains: the numeric and annunciator LED's, 4-to-7 line decoders (IC1, 2 and 5) for the three groups of numeric displays, buffers (IC3 and 4) for the annunciators, and switches (TR1 - 12) for LED anodes (the display is time-shared).

A simplified timing diagram for the fundamental waveforms on pcb's 49 and 50 is shown below.

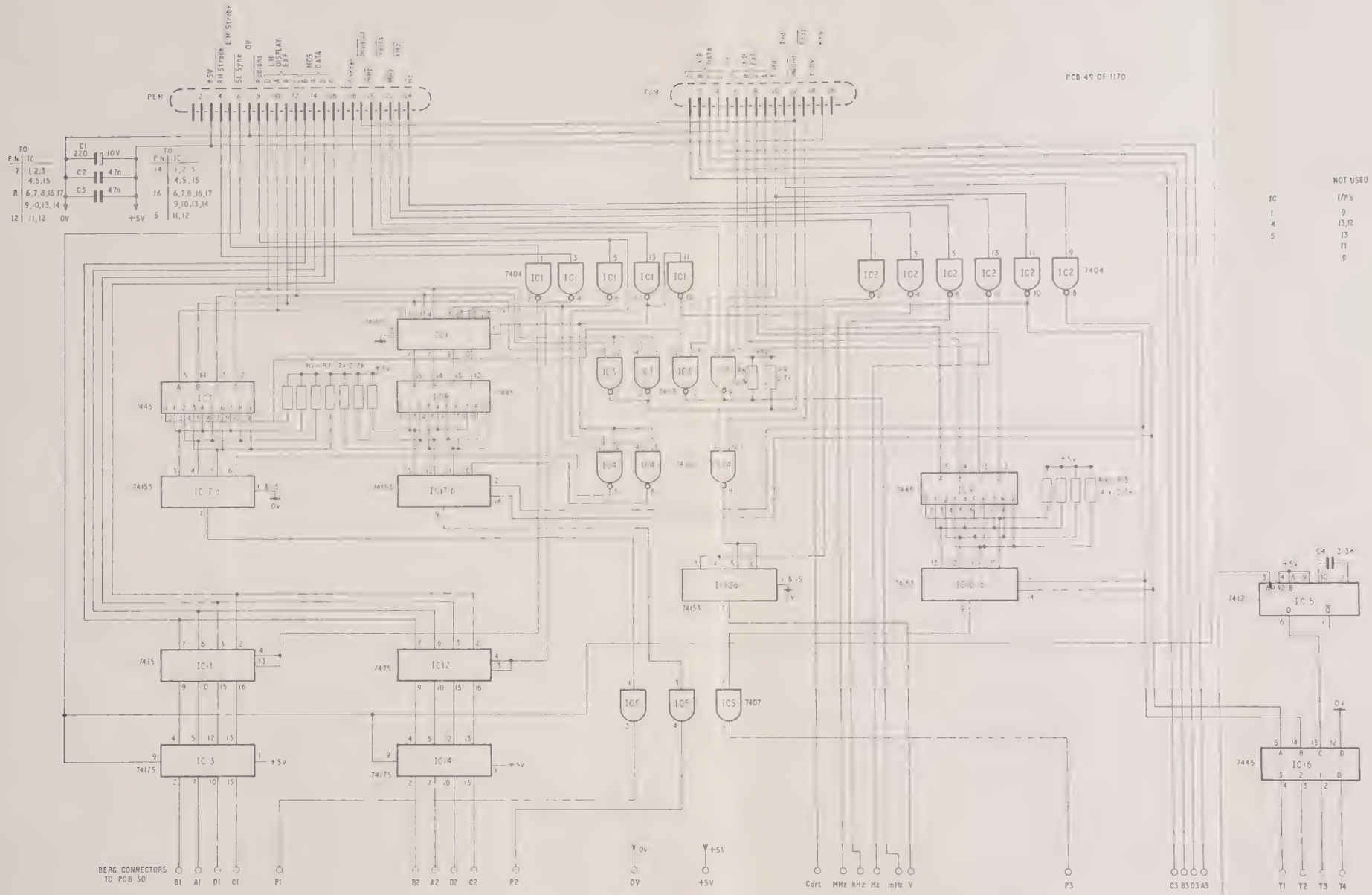


Simplified Timing Diagram for PCB 49/50 Signals.

KB (keyboard) DATA, input to pcb 49 at PLM, is routed directly to decoder IC5 (pcb 50) which controls LED's X7 - X9 (keyboard display). MOS DATA (LH and RH display data), input to pcb 49 at PLN is latched at IC11/12 and IC13/14 (pcb 49) then routed to decoders IC1/2 (pcb 50) which control X1 – X3 and X4 – X6 (LH and RH display)

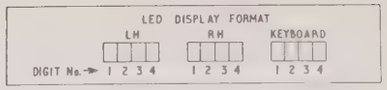
IC11/12 hold updated display data while IC13/14 hold currently displayed data. When the LH and RH STROBE pulses occur (at PLN), the LH and RH updated data is latched into IC11/12. The ST SYNC signal at PLN causes the updated data to be transferred to latches in IC13/14, so replacing the then currently displayed data.

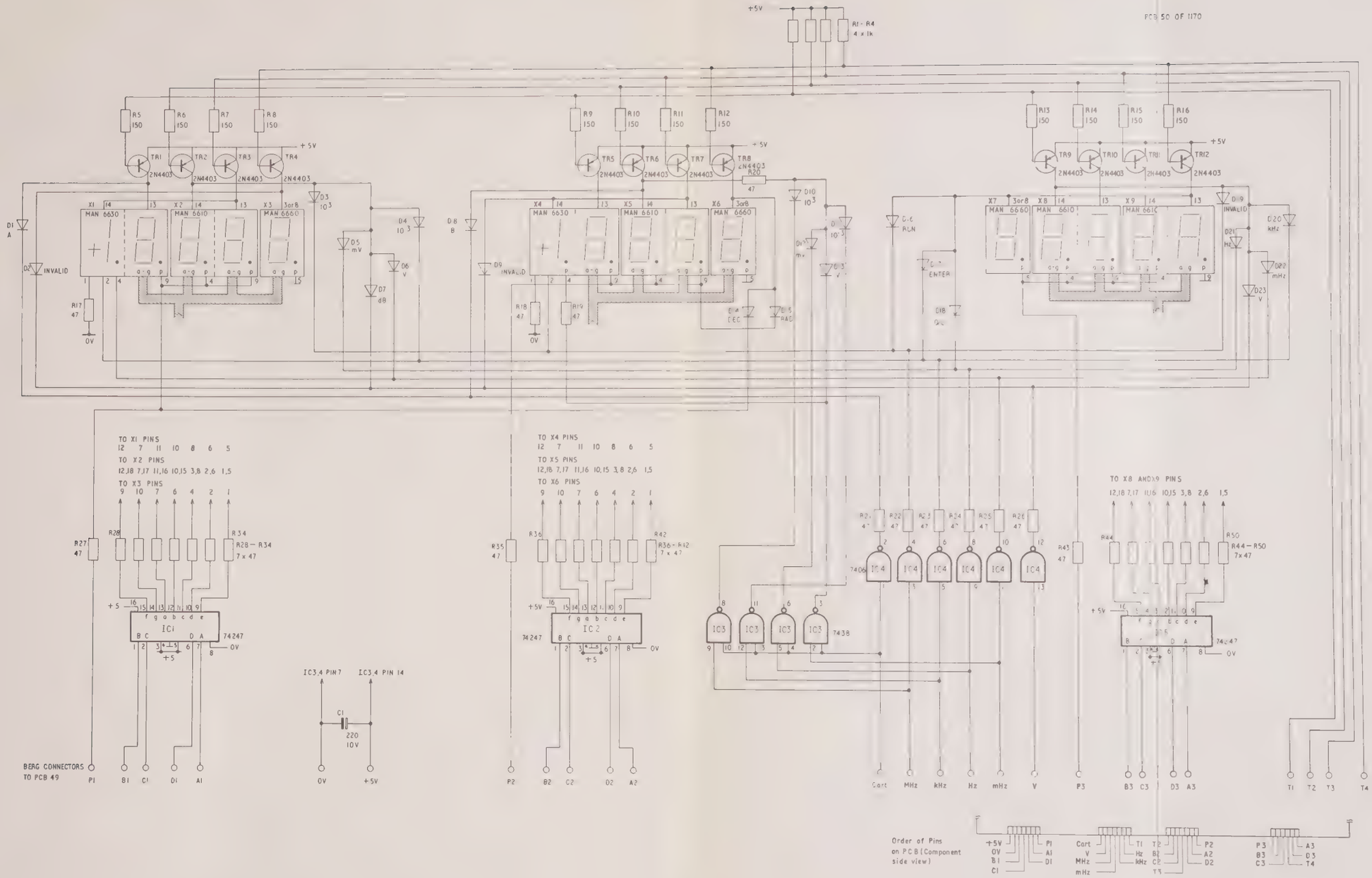
The display is time shared. Digits 1, 2, 3 and 4 are switched-on sequentially; respective digits in all three groups of LED's are switched on simultaneously (i.e. digit 1 is switched-on in all three groups, then digit 2 is switched-on in all three groups etc.). The time sharing is controlled by the T9, T10 inputs (PLM) and monostable (IC15) input to IC16. The monostable output produces a blanking period to prevent display ghosting.



NOT USED

IC	I/P's	O/P's
1	9	8
4	13,12	11
5	13	12
	11	10
	9	8


LED DISPLAY FORMAT
LH
RH
KEYBOARD
DIGIT No.→ 1 2 3 4
1 2 3 4
1 2 3 4


+5V
R1 - R4
4 x 1k
R5 150
R6 150
R7 150
R8 150
TR1 2N4403
TR2 2N4403
TR3 2N4403
TR4 2N4403
+5V
X1 MAN 6630
X2 MAN 6610
X3 3or8 MAN 6660
D1 A
D2 INVALID
D3 10^3
D4 10^3
D5 mV
D6 V
D7 dB
R17 47
0V
R9 150
R10 150
R11 150
R12 150
TR5 2N4403
TR6 2N4403
TR7 2N4403
TR8 2N4403
R20 47
X4 MAN 6630
X5 MAN 6610
X6 3or8 MAN 6660
D8 B
D9 INVALID
D10 10^3
D11 mV
D12 V
D13 DEC
D14 HEX
R18 47
R19 47
R13 150
R14 150
R15 150
R16 150
TR9 2N4403
TR10 2N4403
TR11 2N4403
TR12 2N4403
X7 3or8 MAN 6660
X8 MAN 6610
X9 MAN 6610
D15 RUN
D16 ENTER
D17
D18
D19 INVALID
D20 kHz
D21 Hz
D22 mHz
D23 V
TO X1 PINS
12 7 11 10 8 6 5
TO X2 PINS
12,18 7,17 11,16 10,15 3,8 2,6 1,5
TO X3 PINS
9 10 7 6 4 2 1
R27 47
R28
R34
R28 – R34
7 x 47
IC1
74247
BERG CONNECTORS
TO PCB 49
P1 B1 C1 D1 A1
IC3,4 PIN 7
IC3,4 PIN 14
C1
220
10V
0V
+5V
TO X4 PINS
12 7 11 10 8 6 5
TO X5 PINS
12,18 7,17 11,16 10,15 3,8 2,6 1,5
TO X6 PINS
9 10 7 6 4 2 1
R35 47
R36
R42
R36 – R42
7 x 47
IC2
74247
P2 B2 C2 D2 A2
R21 47
R22 47
R23 47
R24 47
R25 47
R26 47
7406 IC4
IC3 7438
TO X8 AND X9 PINS
12,18 7,17 11,16 10,15 3,8 2,6 1,5
R43 47
R44
R50
R44 – R50
7 x 47
IC5
74247
Cart MHz kHz Hz mHz V
P3 B3 C3 D3 A3
T1 T2 T3 T4
Order of Pins on PCB (Component side view)
+5V 0V B1 C1 P1 A1 D1
Cart V MHz mHz T1 Hz kHz T2 B2 C2 T3 P2 A2 D2
P3 B3 C3 A3 D3 T4

APPENDIX B2 Store State Indicator

TG 1212A Store State Indicator

A 256 bit pulse train generated from the 2MHz, 500kHz and Sync. inputs synchronises with the clock used for the MOS and Latch stores. This pulse train is used to generated strobes which determine the store time-slot selected.

Read

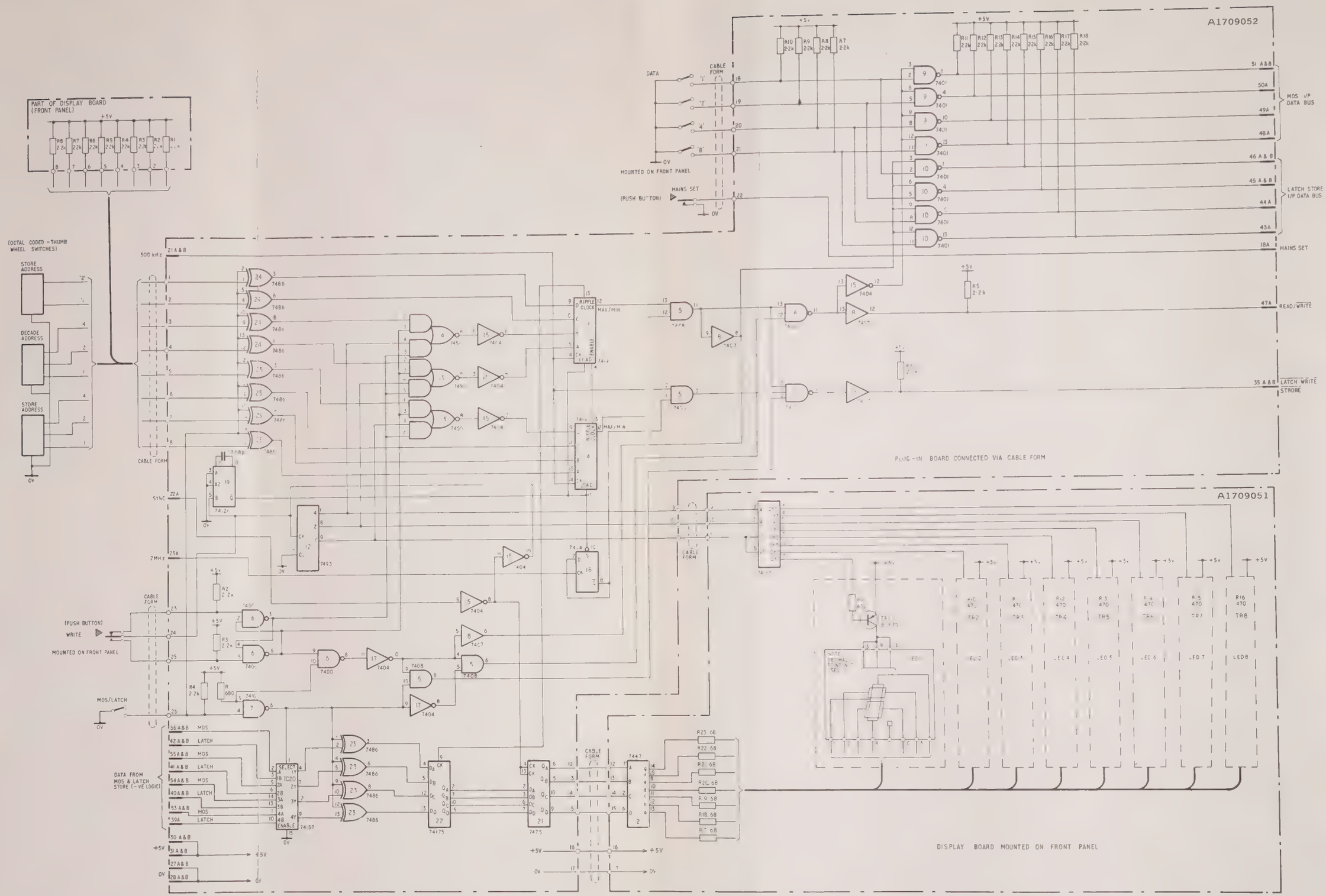
The Sync. pulse starts a pulse train and loads into IC3 and 4 a number selected on the store address switches and a number (0 - 7) from IC12.

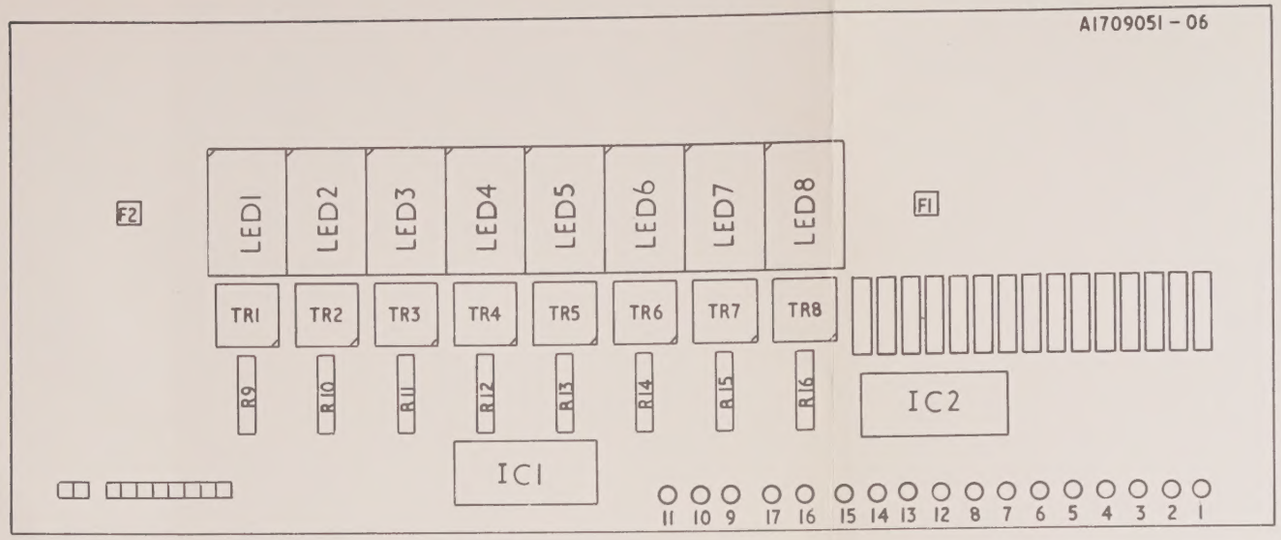
IC3 and 4 then count down at 500kHz until they are empty, when a pulse is passed to IC22 Data on the output busses (MOS or Latch depending on IC20) will be latched into IC21. These data will be displayed, after the next Sync pulse, on the LED selected by IC12 (which also selected the decade address) and IC1.

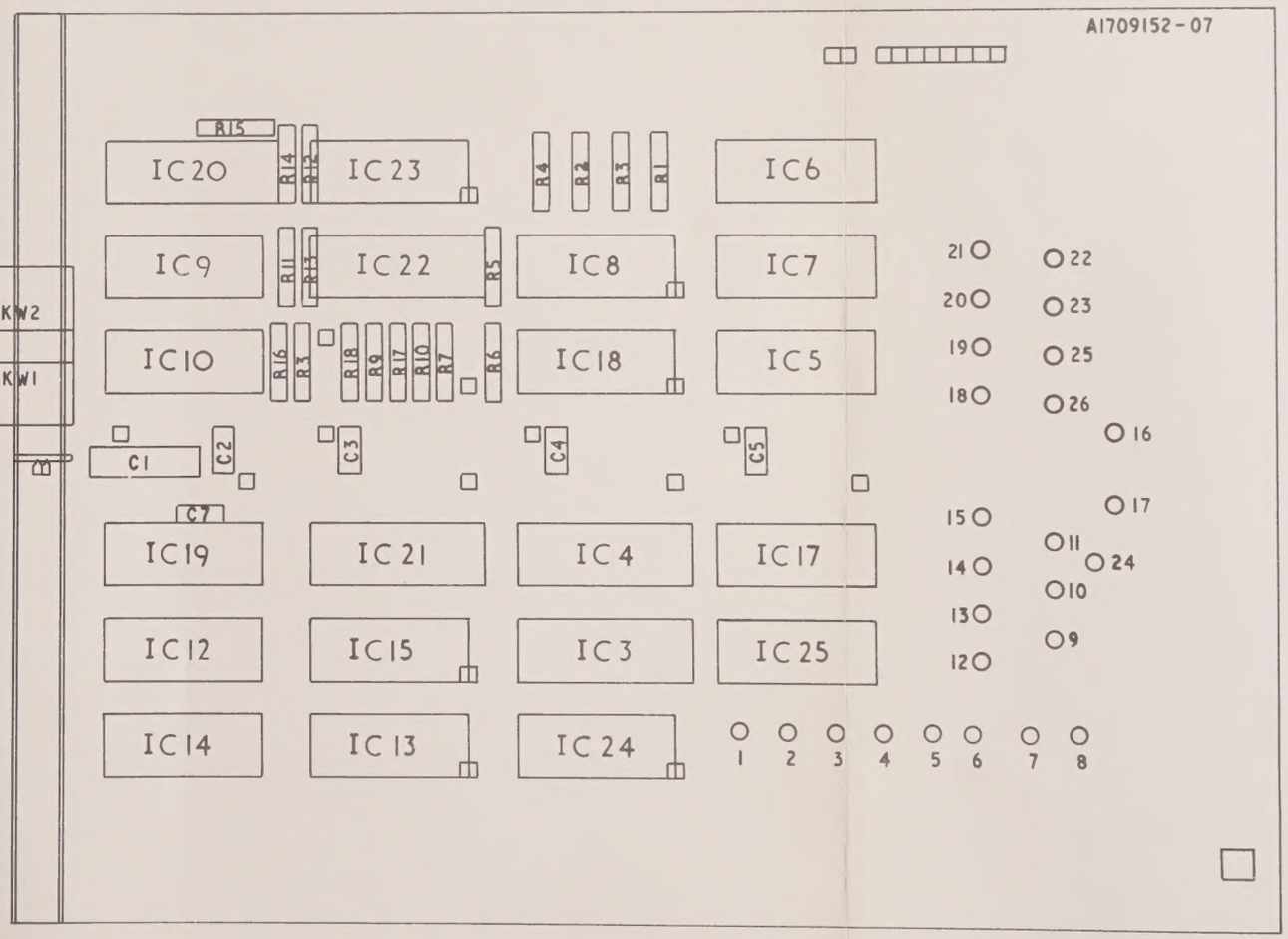
The following pulse train will repeat the action, the decade address having stepped on one count and hence selecting the next store location and LED. The action will repeatedly step through the eight locations of the selected MOS store address, or the two of the Latch store.

Write

Pressing the write button causes bistable IC6 to flip over at the next Sync pulse. The selections of all three octal switches are loaded into IC3 and 4. When the contents of IC3 and 4 reaches zero a write strobe is generated via IC5, 7 and 8 and EC35 and 47A. This will cause the data on the input busses from the data switches to be written into the selected location via IC9 or 10 depending on which is selected.


A1709052
PART OF DISPLAY BOARD (FRONT PANEL)
+5V
R8 2·2k
R7 2·2k
R6 2·2k
R5 2·2k
R4 2·2k
R3 2·2k
R2 2·2k
R1 2·2k
(OCTAL CODED - THUMB WHEEL SWITCHES)
STORE ADDRESS
DECADE ADDRESS
STORE ADDRESS
0V
500 kHz
21 A & B
CABLE FORM
SYNC
22A
2MHz
25A
DATA
CABLE FORM
'1'
'2'
'4'
'8'
18
19
20
21
0V
MOUNTED ON FRONT PANEL
MAINS SET
(PUSH BUTTON)
22
0V
R10 2·2k
R9 2·2k
R8 2·2k
R7 2·2k
R11 2·2k
R12 2·2k
R13 2·2k
R14 2·2k
R15 2·2k
R16 2·2k
R17 2·2k
R18 2·2k
7401
51 A&B
50A
49A
48A
46 A & B
45 A & B
44A
43A
18A
MOS I/P DATA BUS
LATCH STORE I/P DATA BUS
MAINS SET
7404
R5 2·2k
47A
READ/WRITE
35 A & B
LATCH WRITE STROBE
PLUG-IN BOARD CONNECTED VIA CABLE FORM
RIPPLE CLOCK
MAX/MIN
74·2
74·4
74·21
7493
7400
7408
7407
7486
74·57
74175
7447
R2 2·2k
R3 2·2k
R4 2·2k
R 680
(PUSH BUTTON)
WRITE
MOUNTED ON FRONT PANEL
MOS/LATCH
56 A&B MOS
42 A&B LATCH
55 A&B MOS
41 A&B LATCH
54 A&B MOS
40 A&B LATCH
53 A&B MOS
39A LATCH
30 A&B
31 A&B
27 A&B
28 A&B
DATA FROM MOS & LATCH STORE (-VE LOGIC)
R23 68
R22 68
R21 68
R20 68
R19 68
R18 68
A1709051
R1C 47k
R 47K
R2 470
R3 470
R4 470
R5 470
R16 470
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
LED 1
LED 2
LED 3
LED 4
LED 5
LED 6
LED 7
LED 8
DISPLAY BOARD MOUNTED ON FRONT PANEL


A1709051 - 06
F2
F1
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
R9
R10
R11
R12
R13
R14
R15
R16
IC2
IC1
11 10 9 17 16 15 14 13 12 8 7 6 5 4 3 2 1


A1709152 - 07
R15
IC20
R14
R12
IC23
R4
R2
R3
R1
IC6
IC9
R11
R13
IC22
R5
IC8
IC7
KW2
KW1
IC10
R16
R3
R18
R9
R17
R10
R7
R6
IC18
IC5
C1
C2
C3
C4
C5
C7
IC19
IC21
IC4
IC17
IC12
IC15
IC3
IC25
IC14
IC13
IC24
21 22 20 23 19 25 18 26 16 17 15 11 24 14 10 13 9 12
1 2 3 4 5 6 7 8

MP MASTER
MA24246

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